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POWER AND CLOCK GATING MODELLING IN COARSE GRAINED RECONFIGURABLE SYSTEMS

ACM International Conference on
Computing Frontiers 2016

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OUTLINE

- Problem Statement
- Background
 - Dataflow Model of Computation
 - Coarse Grain Reconfiguration
 - Multi-Dataflow Composer Tool
- Proposed approach
 - Parameters Analysis
 - Power Estimation Model
 - Logic Regions Analysis
- Methodology assessment
- Conclusions

PROBLEM STATEMENT

Consumers need:



PROBLEM STATEMENT

Consumers need:

- Integrated complex and fancy resource-intensive applications



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Possible solutions:



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Possible solutions:

- **Dataflow Model of Computation**
 - Modularity and parallelism →
→ **INTEGRATION AND RE-USABILITY**

PROBLEM STATEMENT

Consumers need:

- Integrated complex and fancy resource-intensive applications
- Long battery life



Possible solutions:

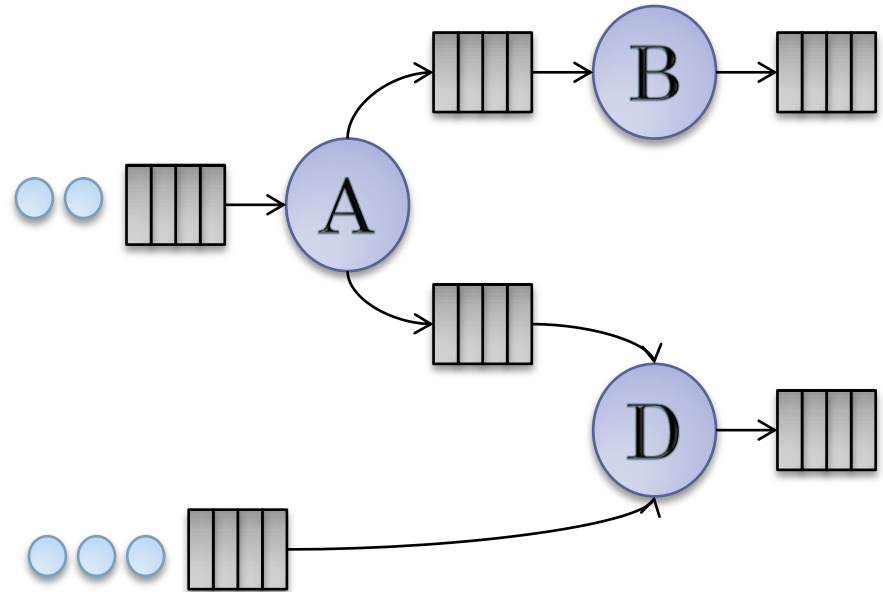
- **Dataflow Model of Computation**
 - Modularity and parallelism →
→ **INTEGRATION AND RE-USABILITY**
- **Coarse-graine reconfiguration**
 - Flexibility and resource sharing →
→ **MULTI-APPLICATION PORTABLE DEVICES**

BACKGROUND

Dataflow Model of Computation

○ DATAFLOW FORMALISM

- Directed graph of **actors** (functional units).
- Actors exchange **tokens** (data packets) through **dedicated channels**

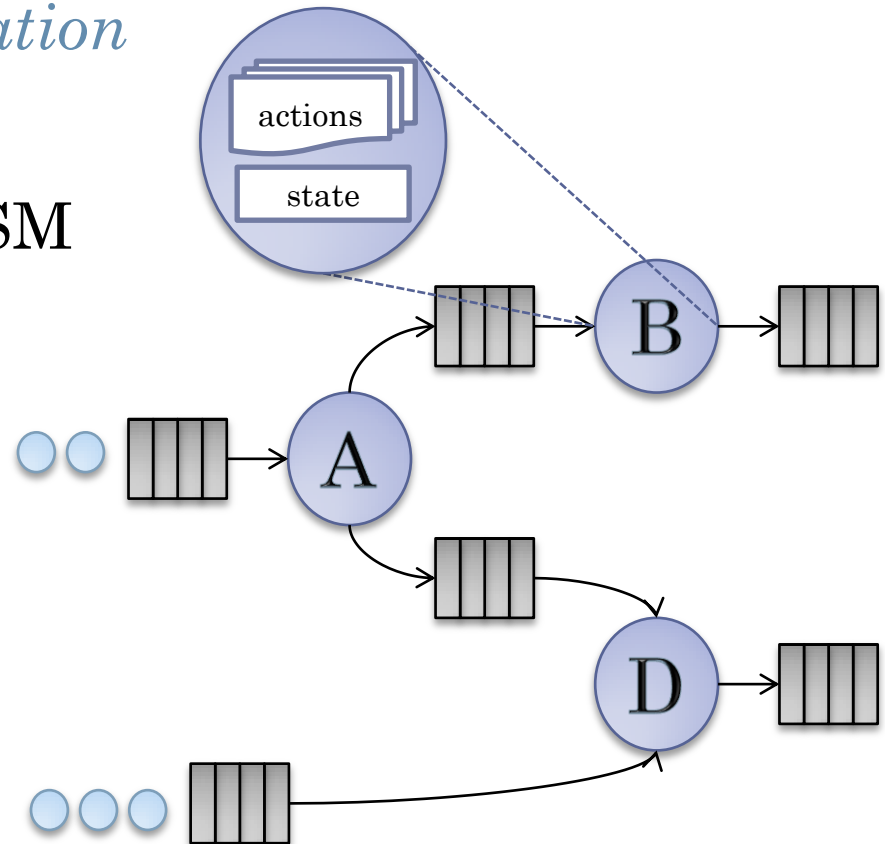


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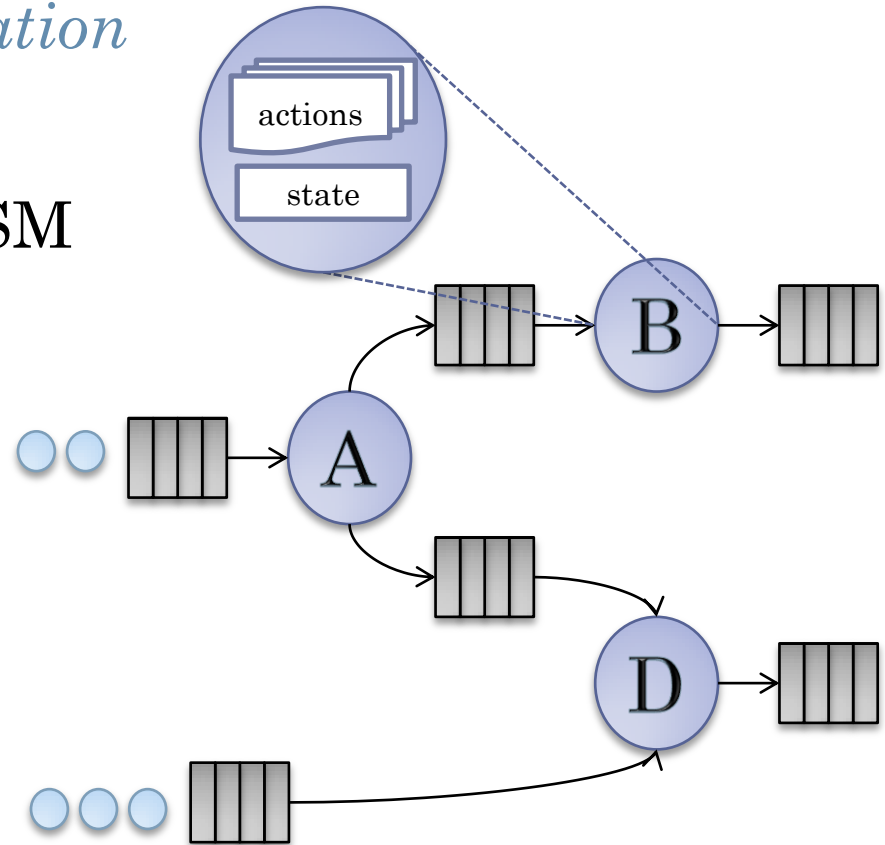


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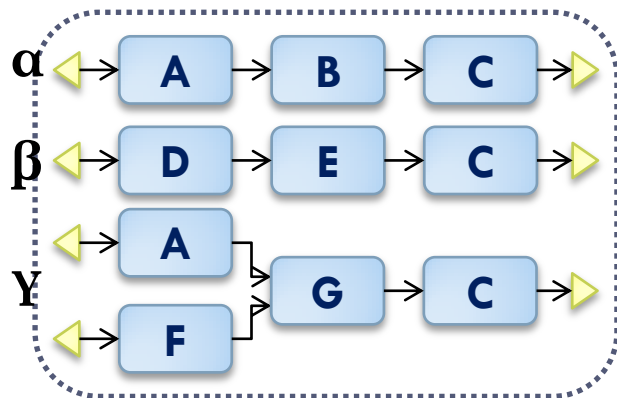


○ CHARACTERISTICS

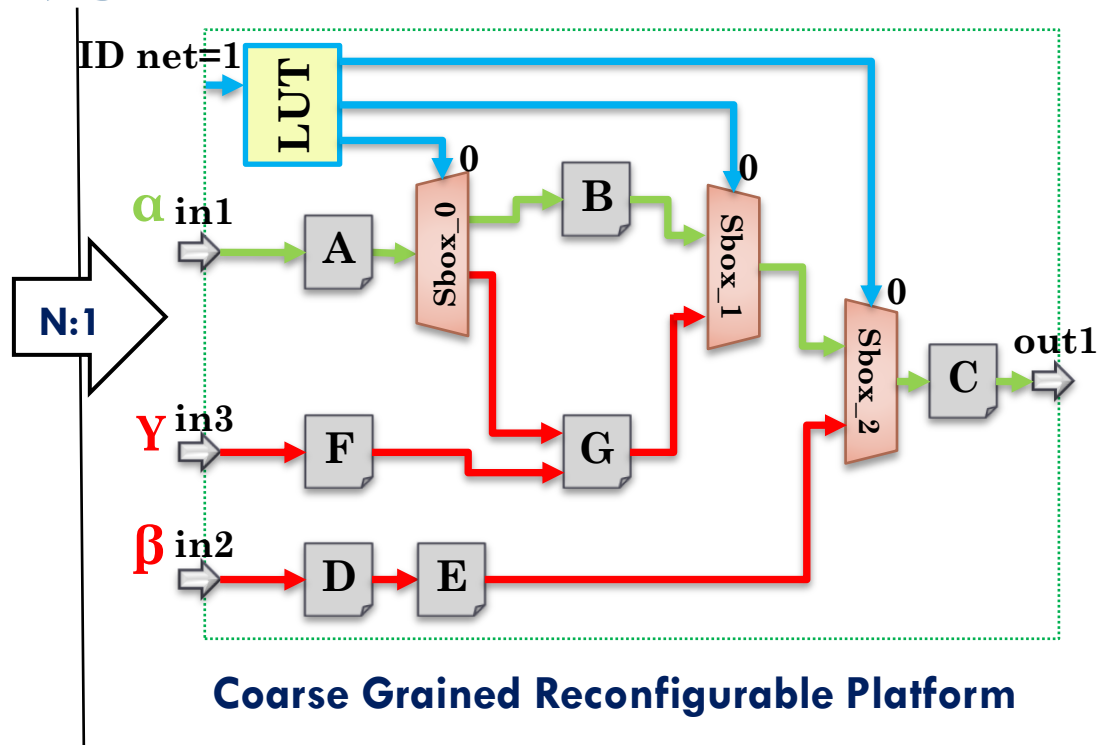
- Explicit the intrinsic application **parallelism**.
- Modularity favours model **re-usability/adaptivity**.

BACKGROUND

Coarse-Graine Reconfiguration



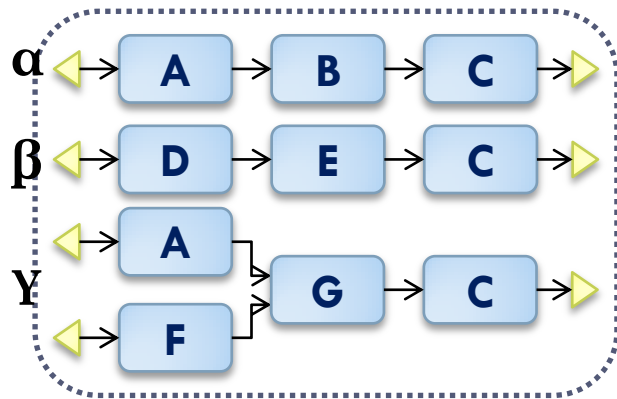
Dataflow Descriptions



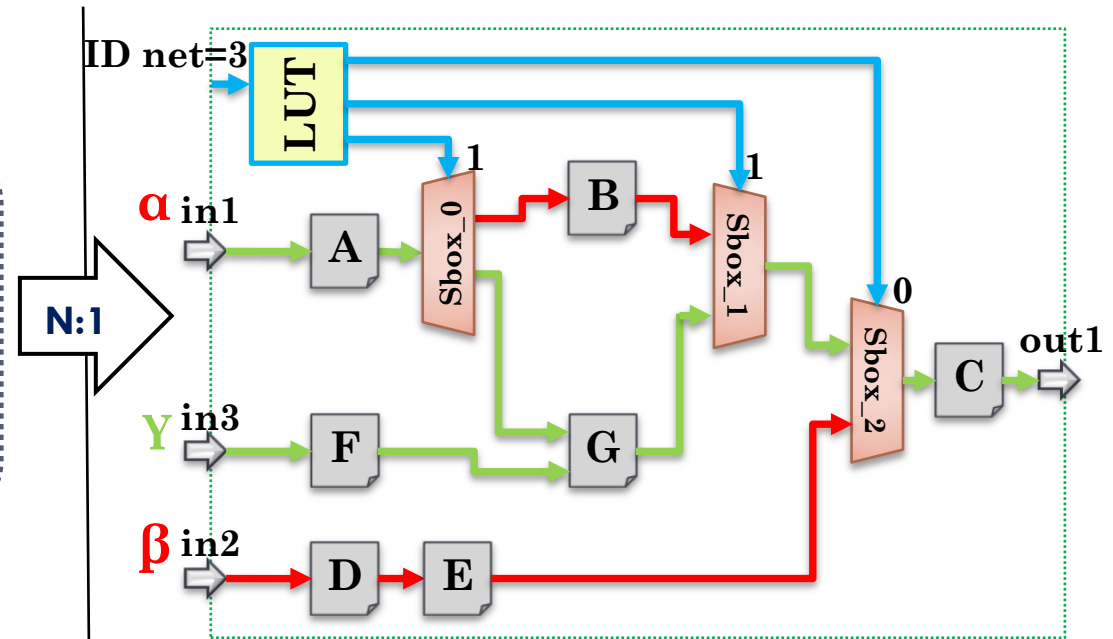
Coarse Grained Reconfigurable Platform

BACKGROUND

Coarse-Graine Reconfiguration



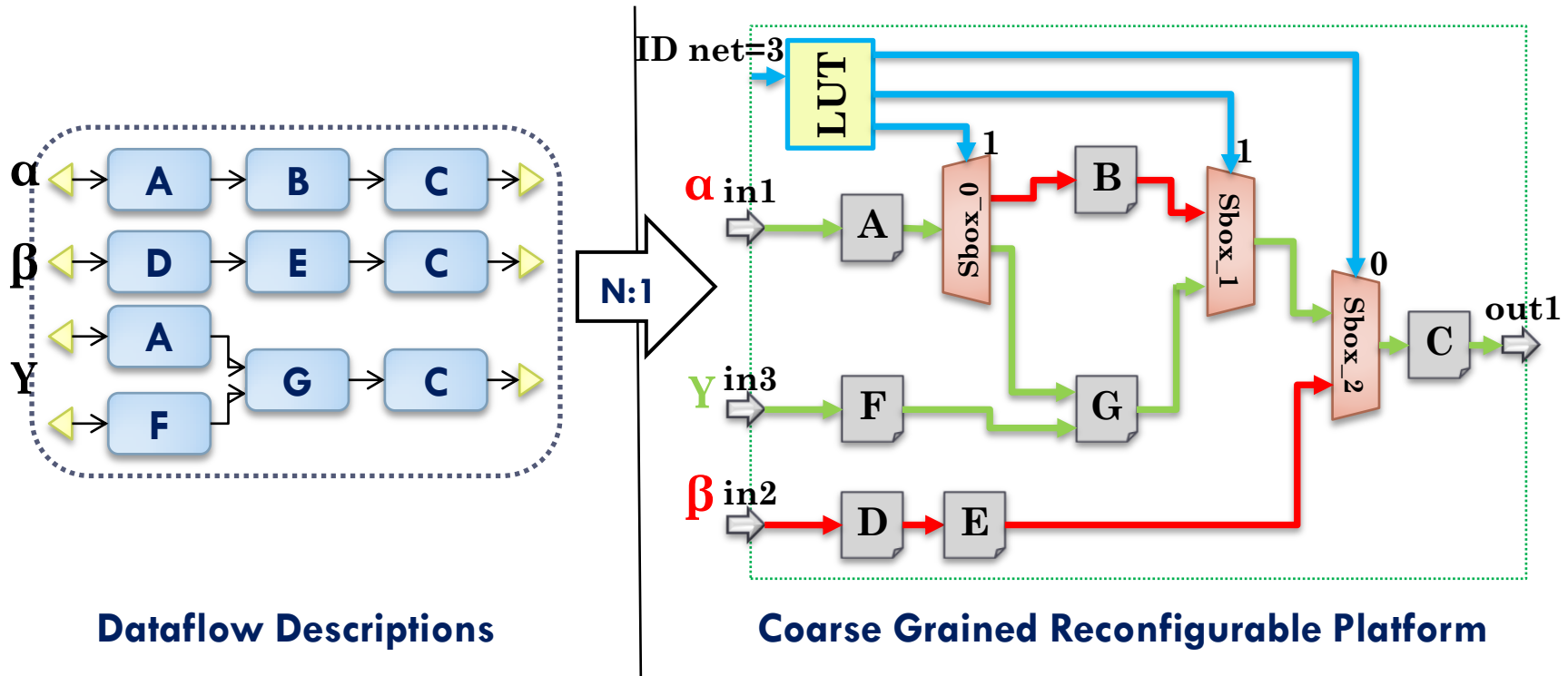
Dataflow Descriptions



Coarse Grained Reconfigurable Platform

BACKGROUND

Coarse-Graine Reconfiguration

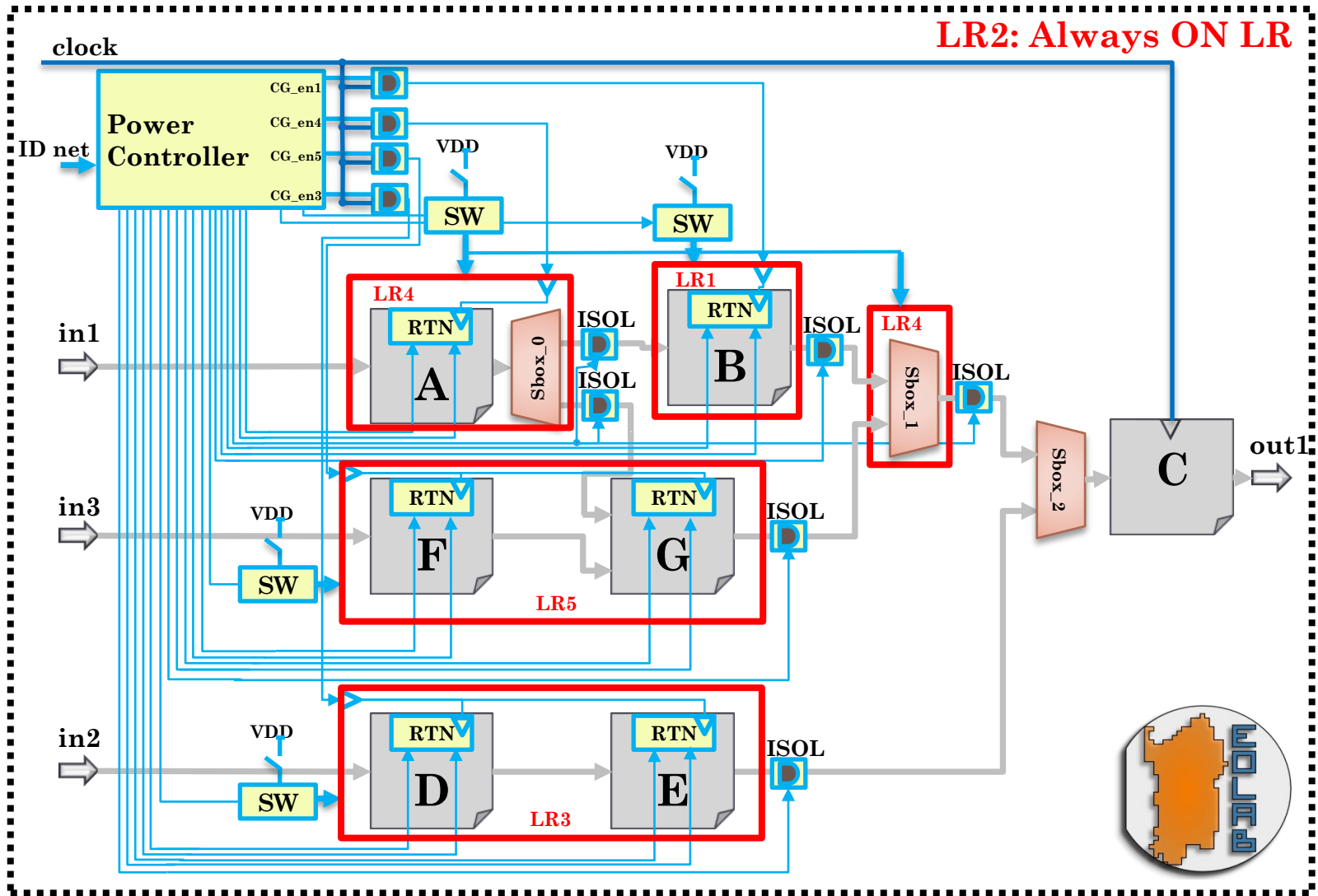


- Large Power consumption → Power Saving Methodologies
 - Dynamic → Clock-gating
 - Static → Power-gating

BACKGROUND

Multi-Dataflow Composer Tool

<http://sites.unica.it/rpct/>



PROPOSED APPROACH

Parameters analysis:

PROPOSED APPROACH

Parameters analysis:

- Architectural parameters

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 - Actors
 - RAMs
 - Combinatorial Logic
 - Sequential Logic...

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 - LR's Activation Time

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PROPOSED APPROACH

Parameters analysis:

- Architectural parameters
 - Actors
 - RAMs
 - Combinatorial Logic
 - Sequential Logic...
- Functional parameters
 - Input Data
 - LR's Activation Time
- Technological parameters
 - As transistors get smaller the contribution of the static contribute gets larger and not negligible.

PROPOSED APPROACH

Power Estimation Model

- Power gating.

$$\begin{aligned} P(LR_i) &= P_{ON}(LR_i) + Ext_Over(LR_i) = \\ &= \sum_{actors \in LR_i} [P(cmb) + P(RC) * \#rtn + P(reg) * (\#reg - \#rtn) / \#reg] * T_{iON} + \\ &+ [P(ISO_{ON}) * \#iso * T_{iON} + P(ISO_{OFF}) * \#iso * T_{iOFF}] + \\ &+ [P(Contr_{ON}) * T_{iON} + P(Contr_{OFF}) * T_{iOFF}] + \\ &+ [P(CG_{ON}) * T_{iON} + P(CG_{OFF}) * T_{iOFF}] \end{aligned}$$

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Power Estimation Model

Standard Cost
Combinational
Logic

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PROPOSED APPROACH

Power Estimation Model

Standard Cost

Combinational
Logic

Sequential
Logic

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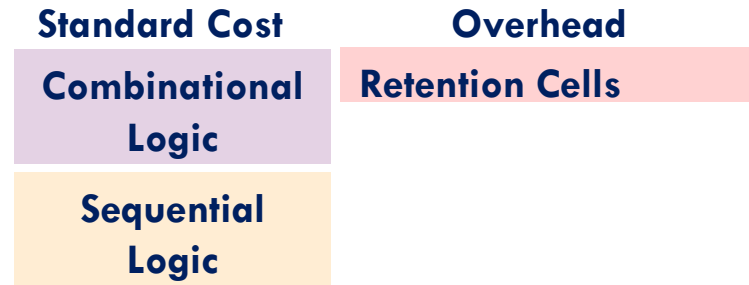
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Power Estimation Model



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PROPOSED APPROACH

Power Estimation Model

Standard Cost	Overhead
Combinational Logic	Retention Cells
Sequential Logic	Isolation Cells

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PROPOSED APPROACH

Power Estimation Model

Standard Cost	Overhead
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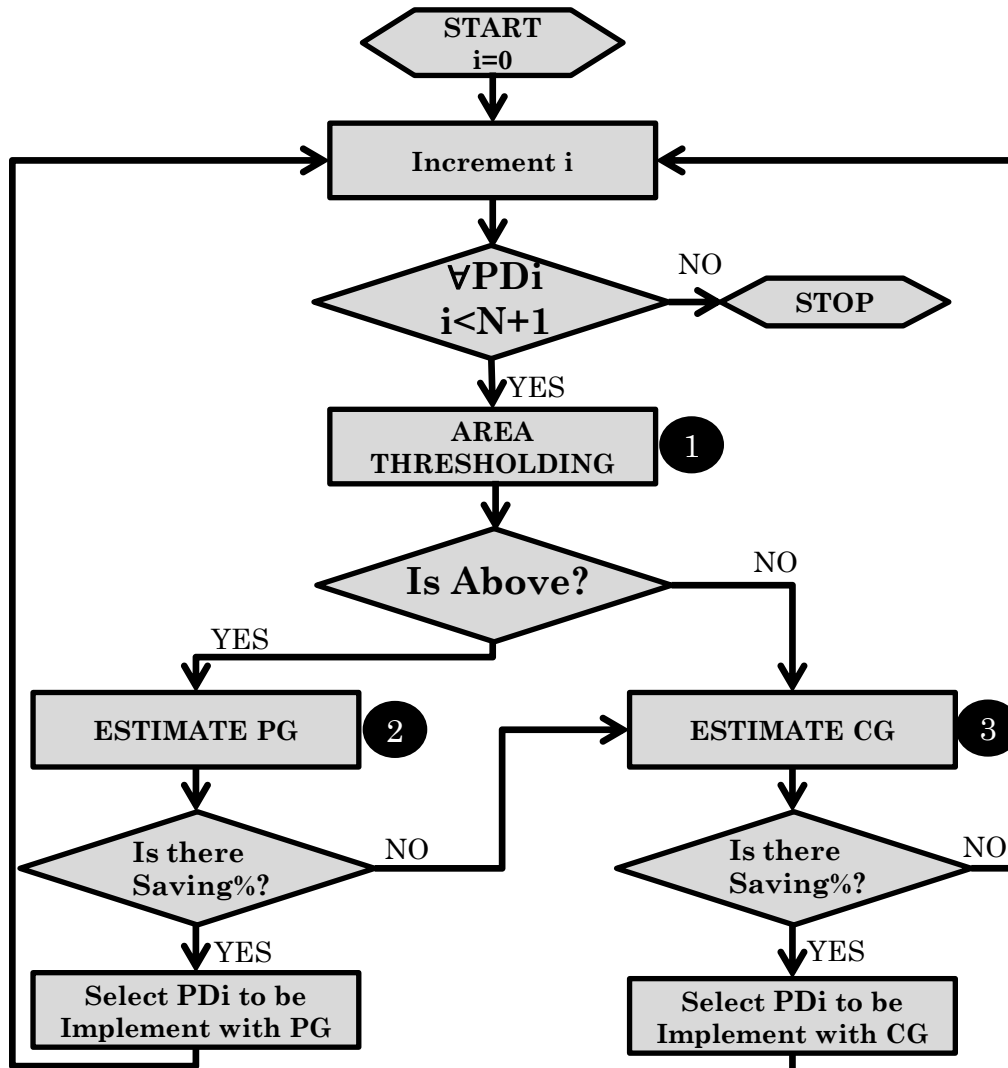
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Term not present
in CG static model!

PROPOSED APPROACH

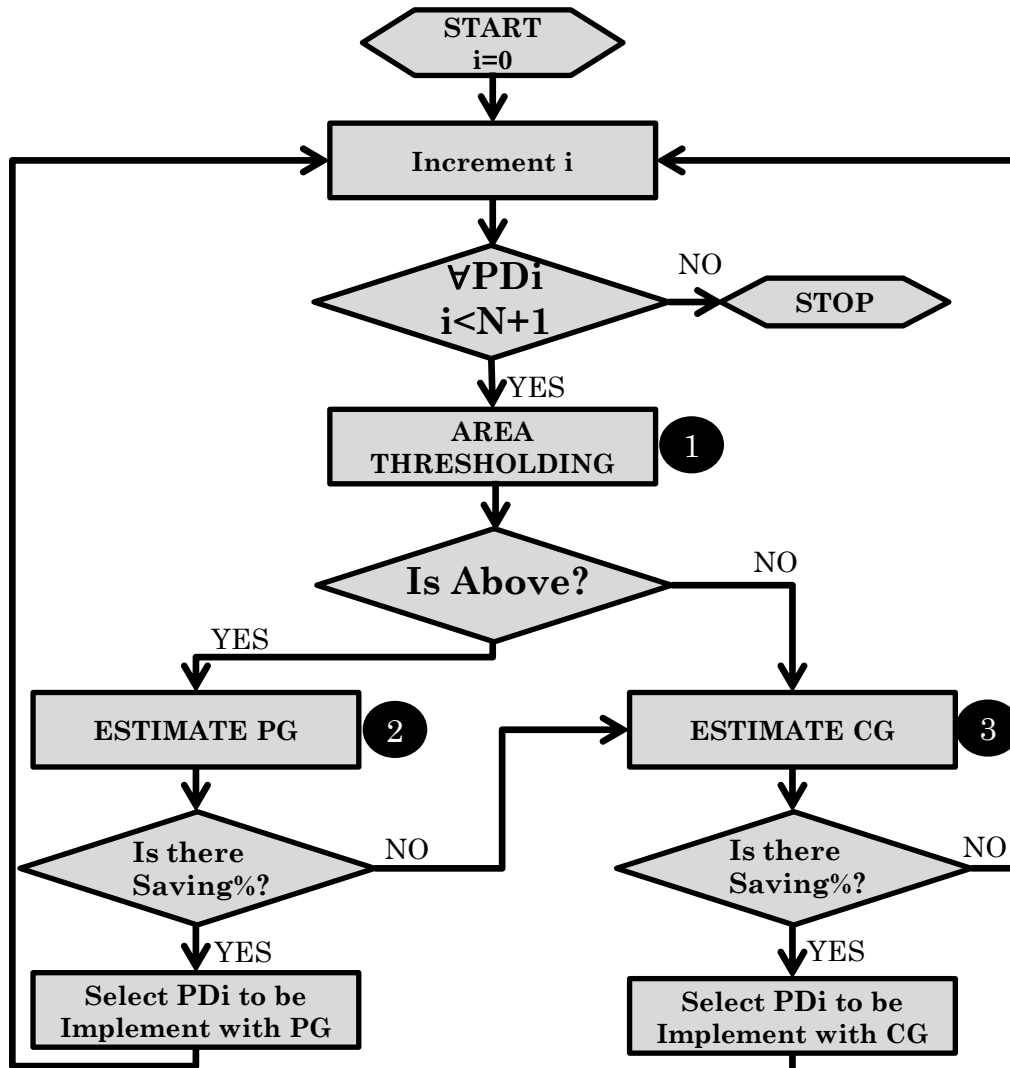
LRs analysis



PROPOSED APPROACH

LRs analysis

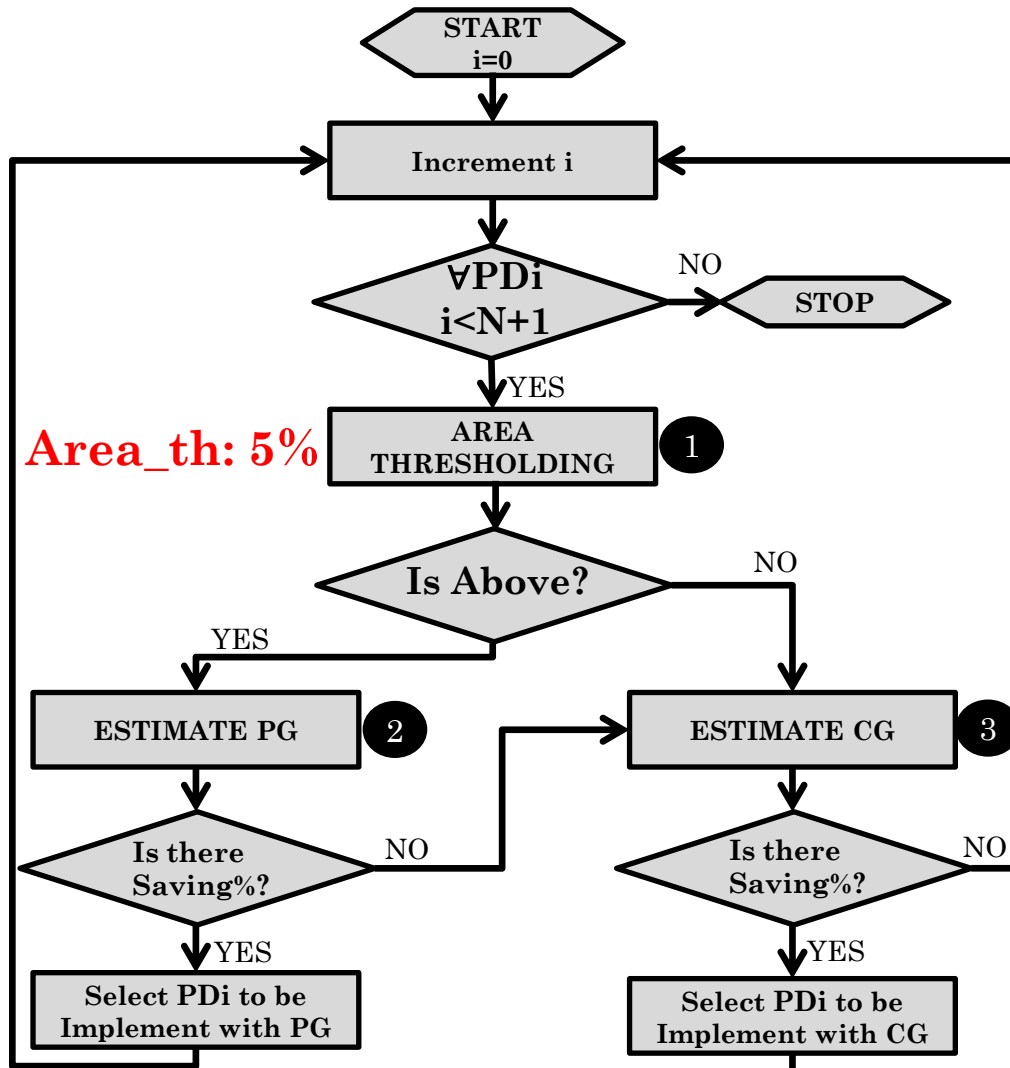
LRs	LR1	LR2	LR3
Area	2%	5.8%	23%
PG	---	+2%	-18%
CG	+1%	-5%	---



PROPOSED APPROACH

LRs analysis

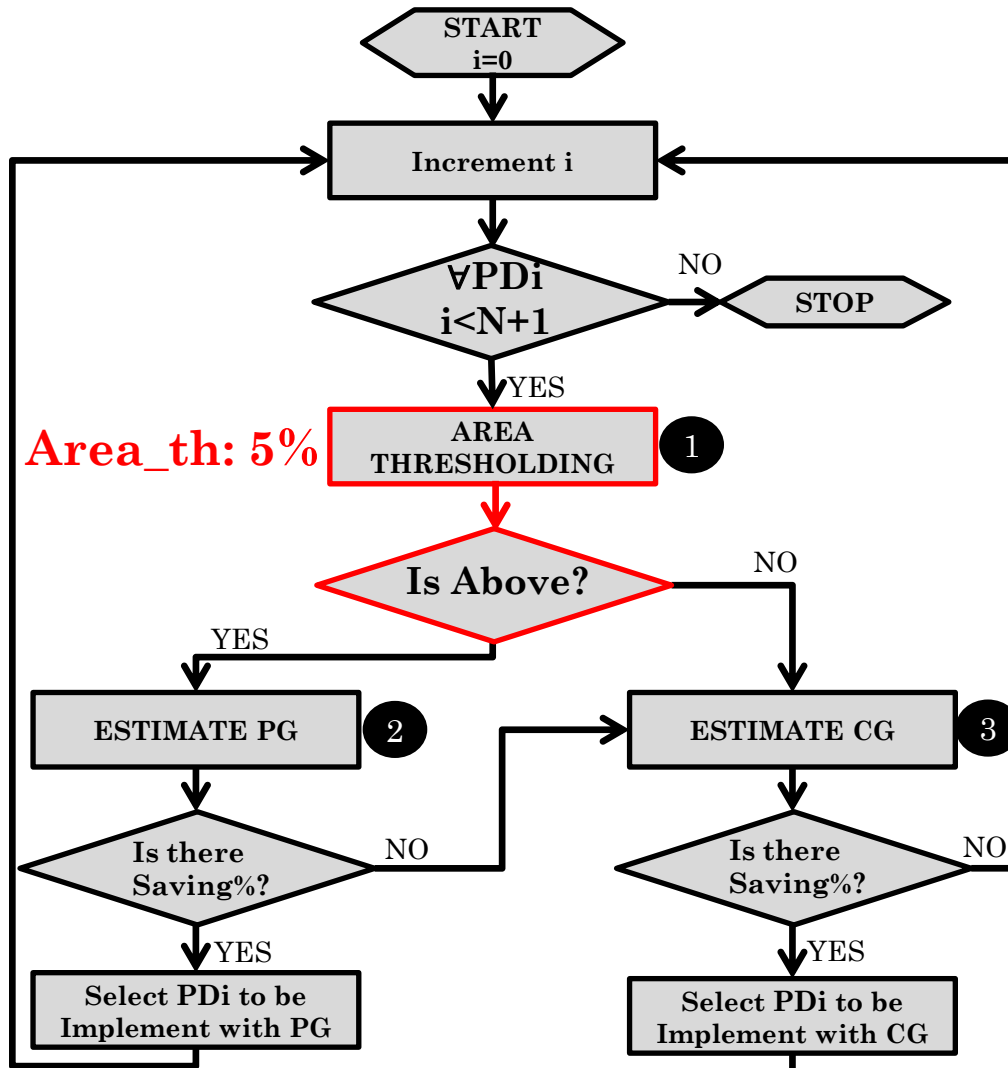
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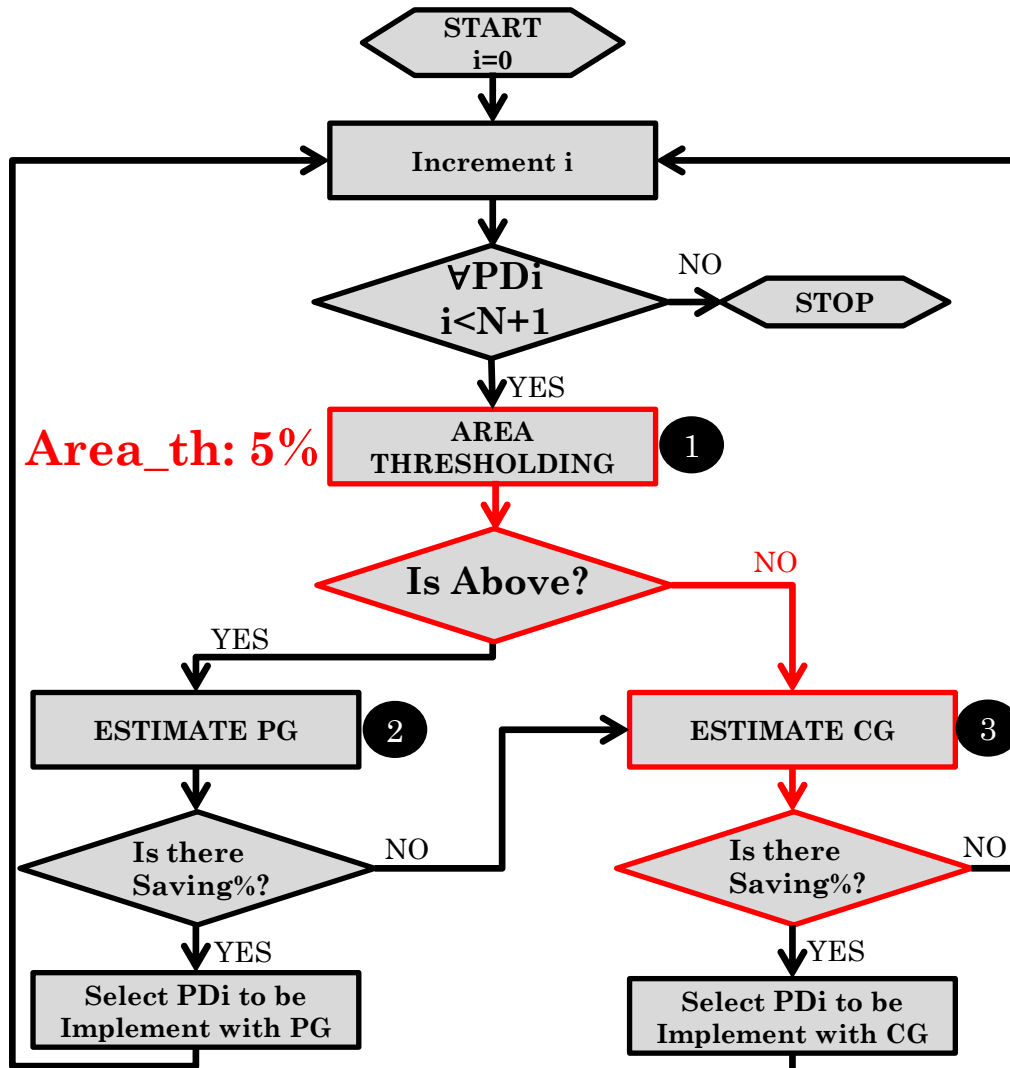


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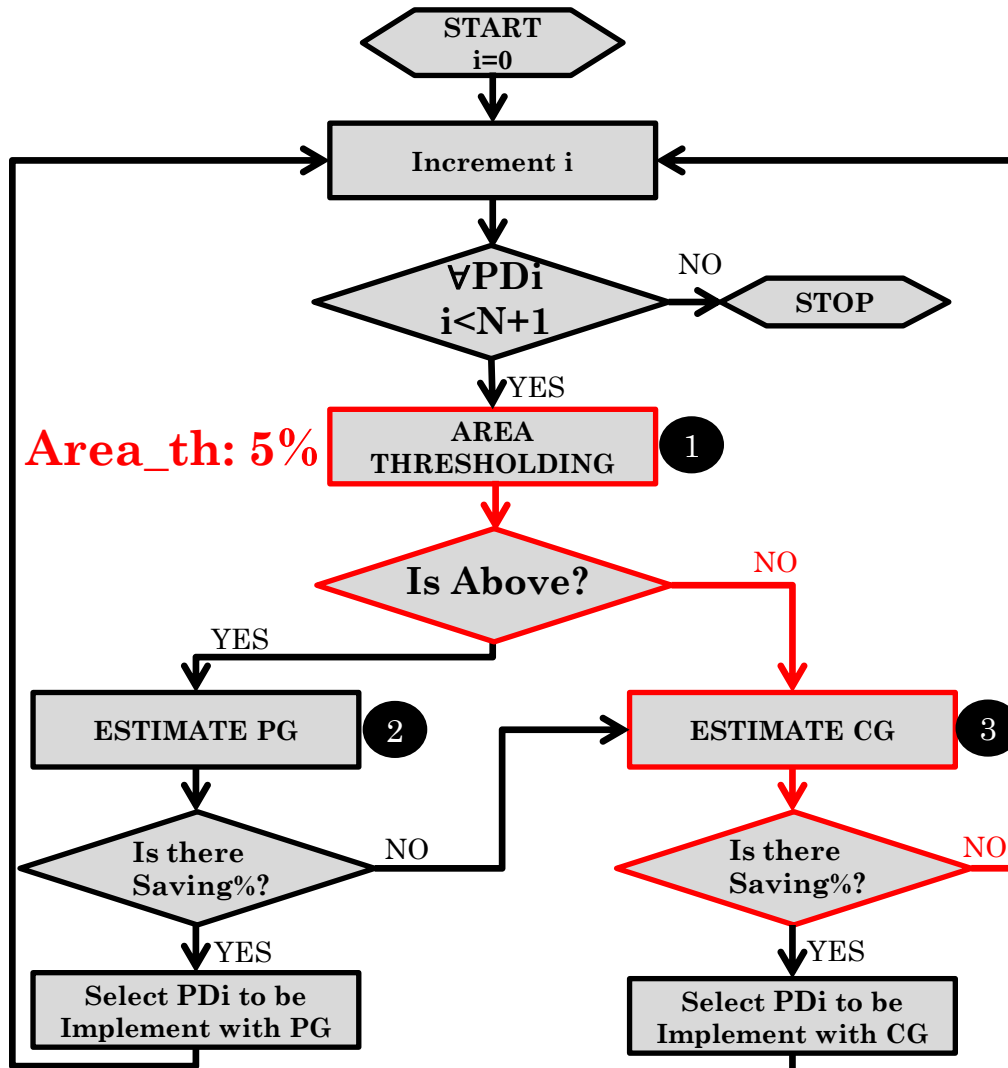


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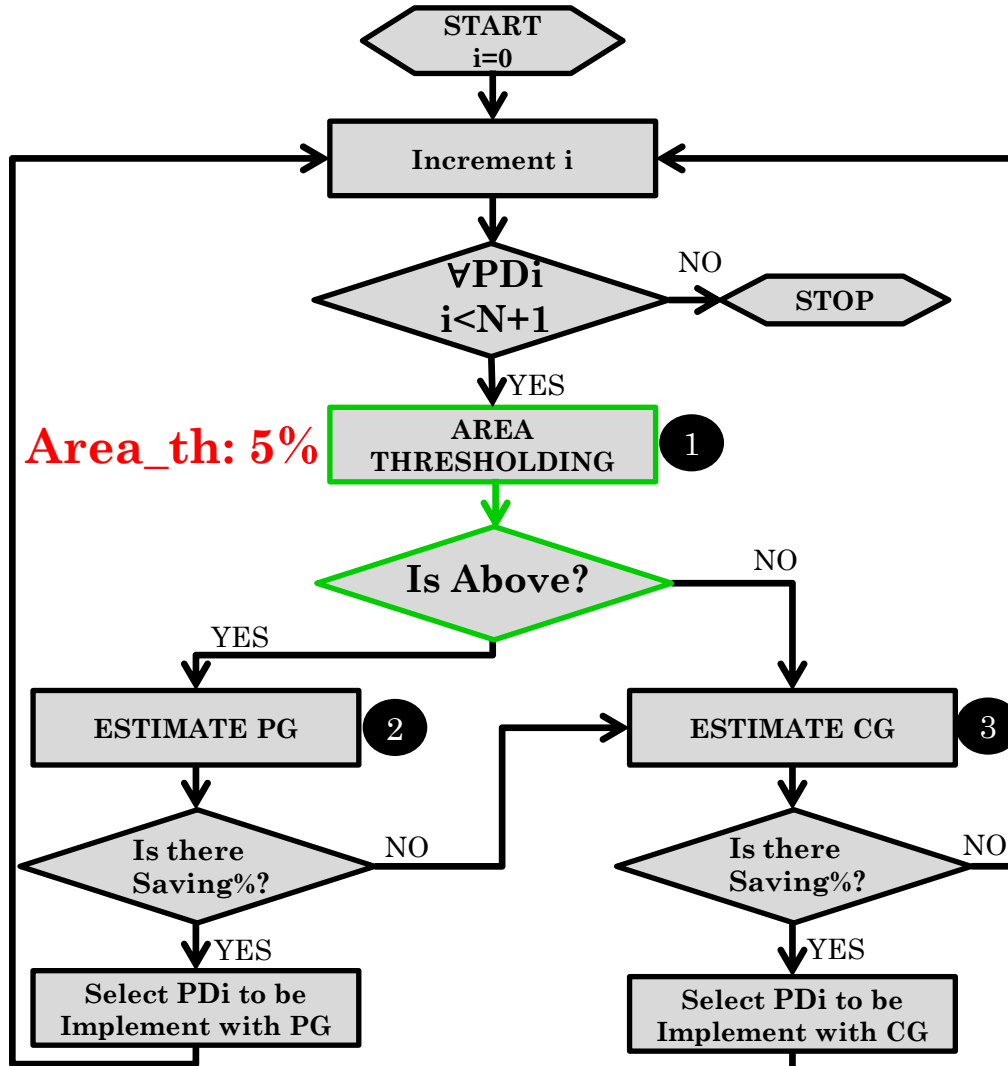


PROPOSED APPROACH

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Area_th: 5%

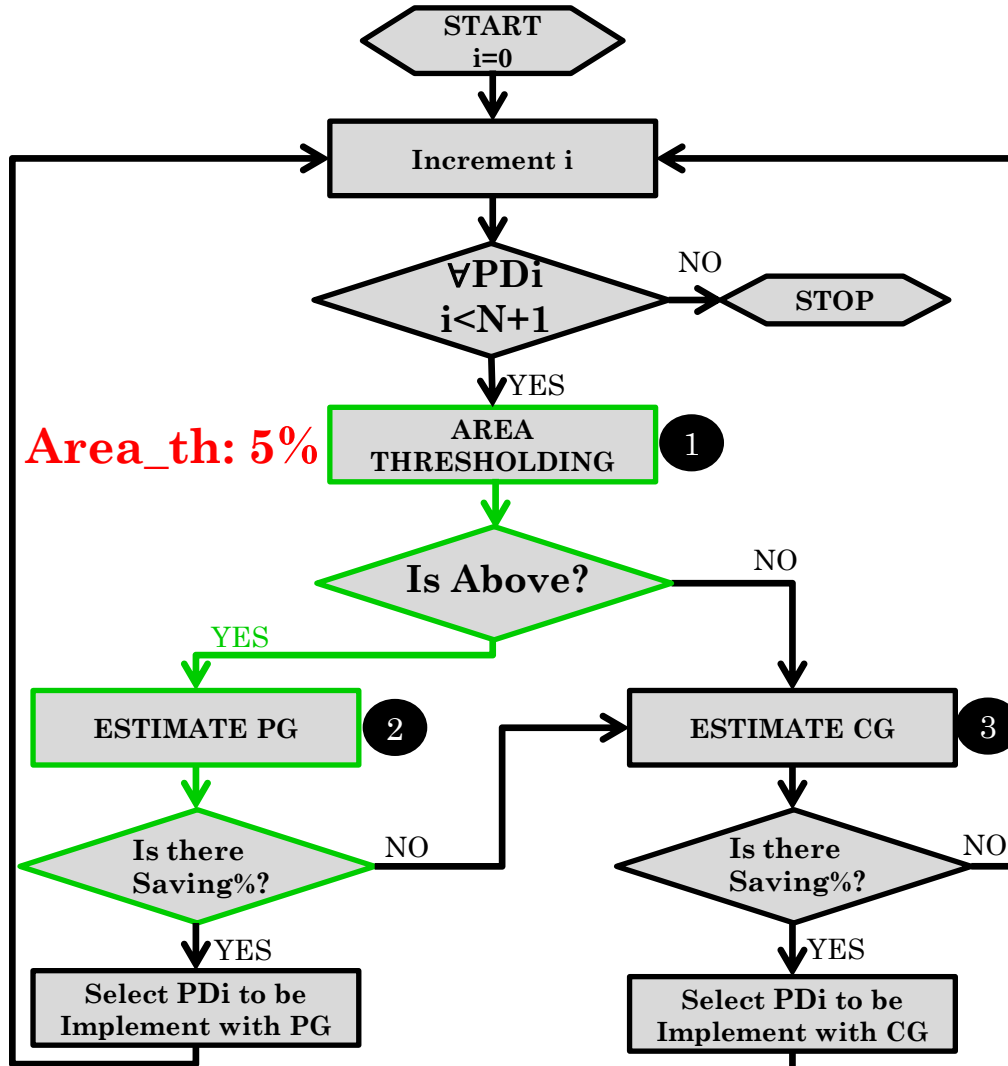
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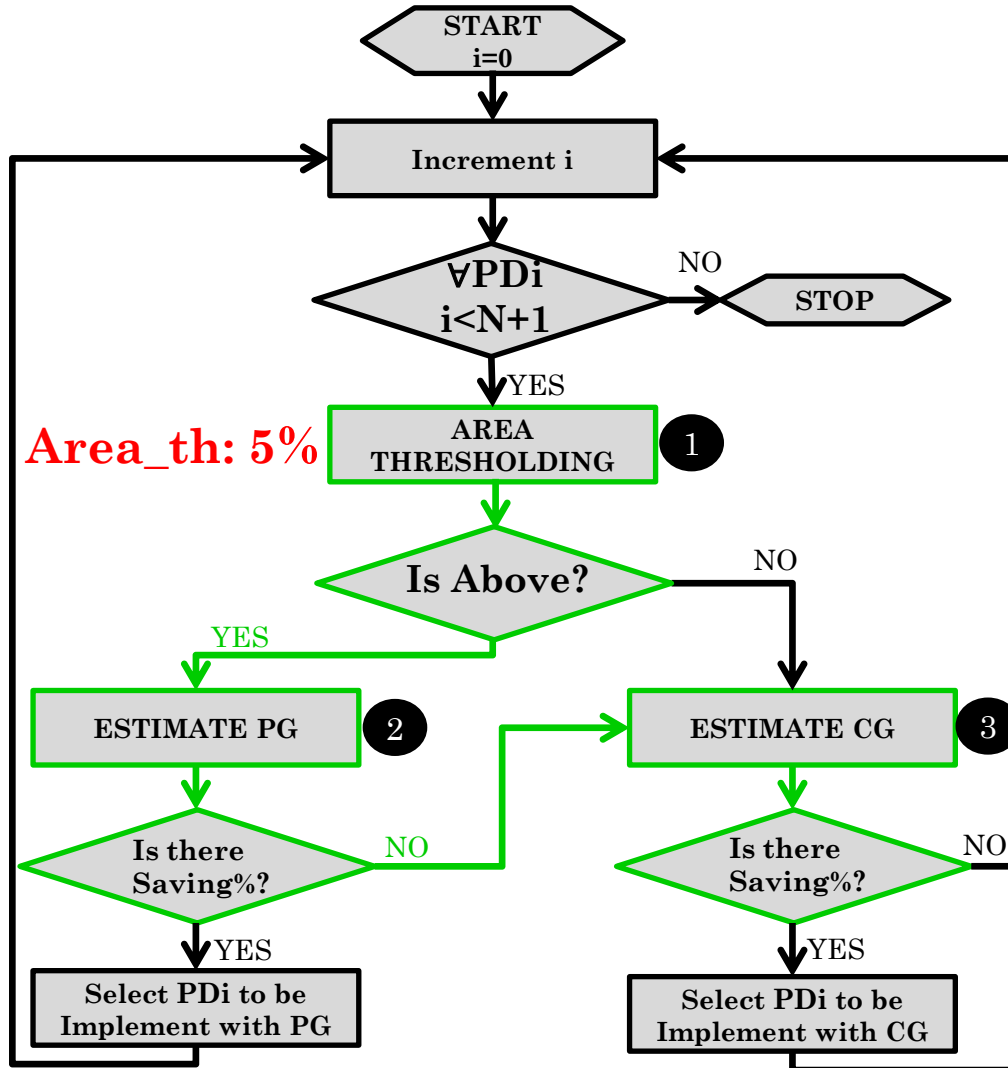
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 Power PG: +2% → Evaluate CG



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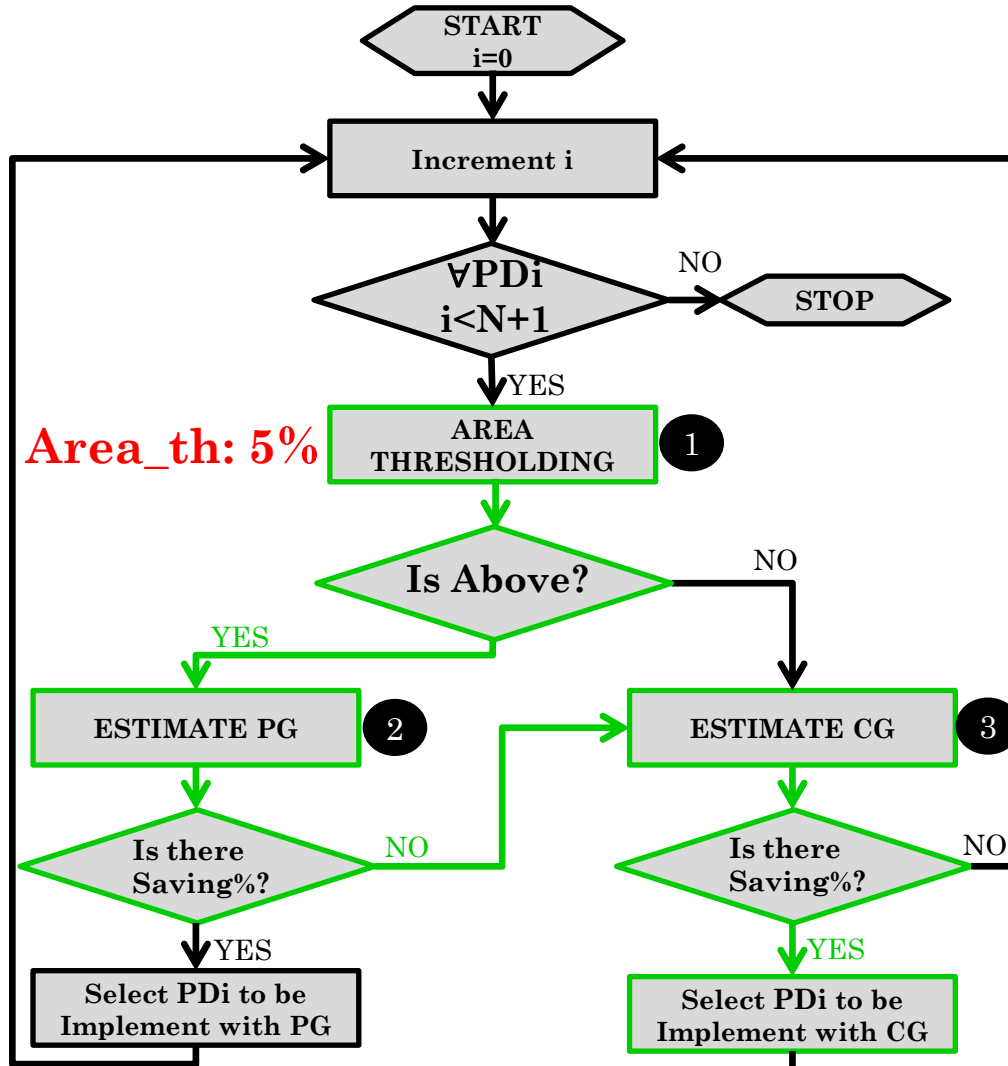
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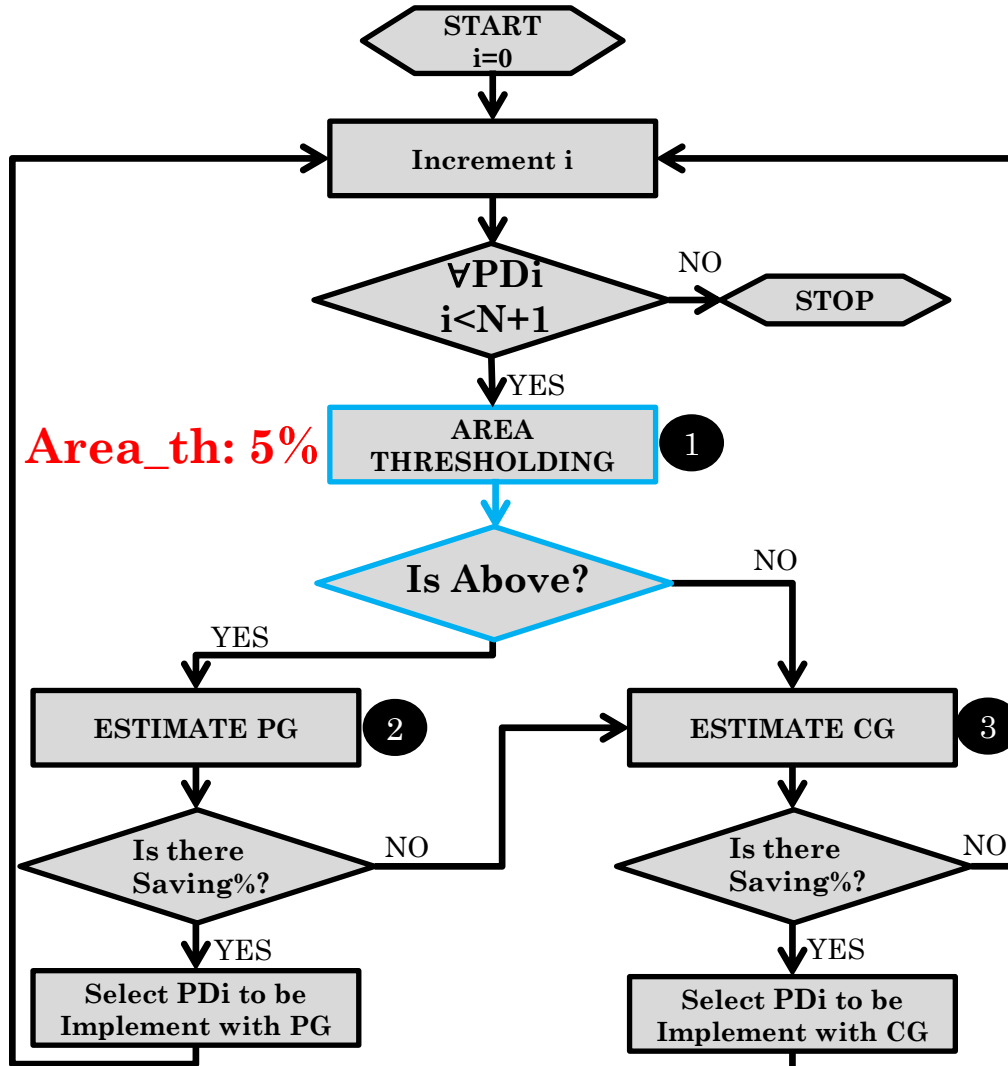
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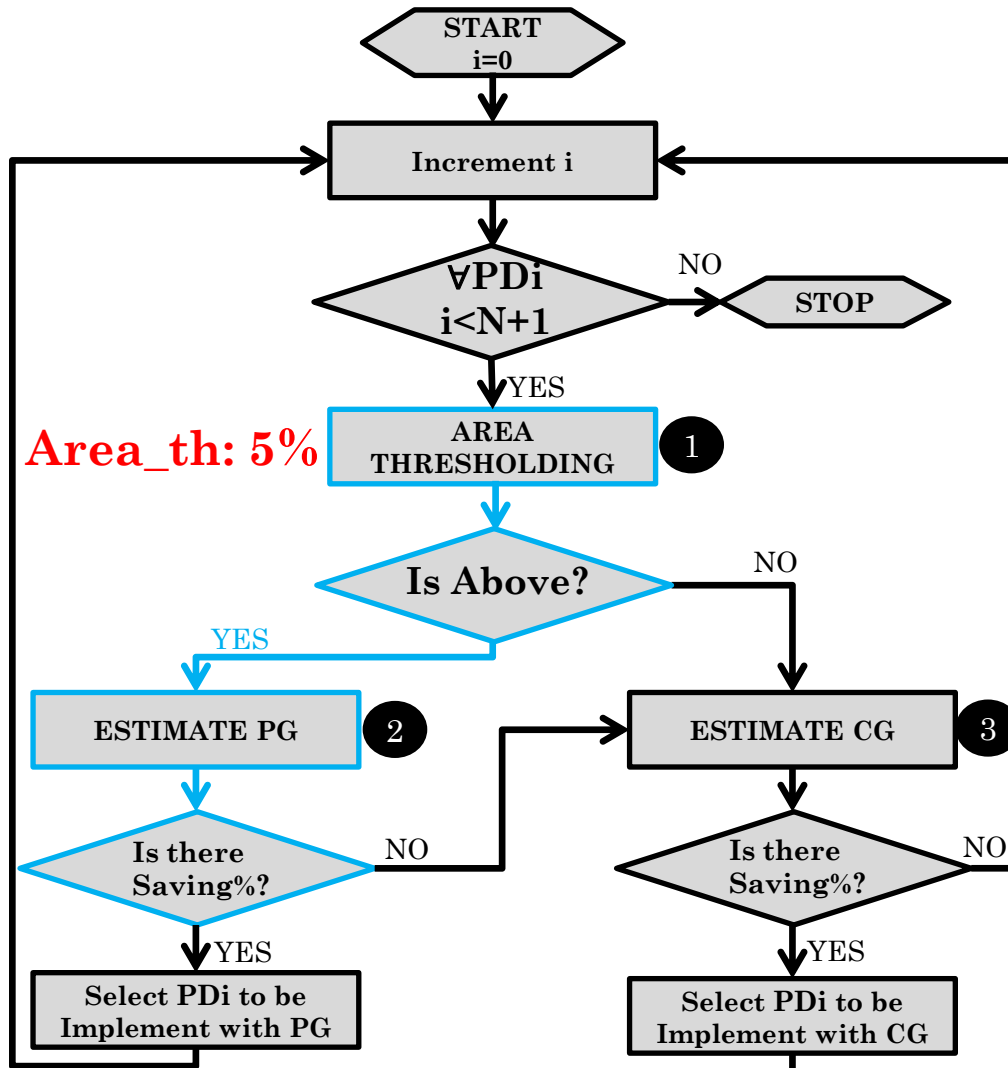
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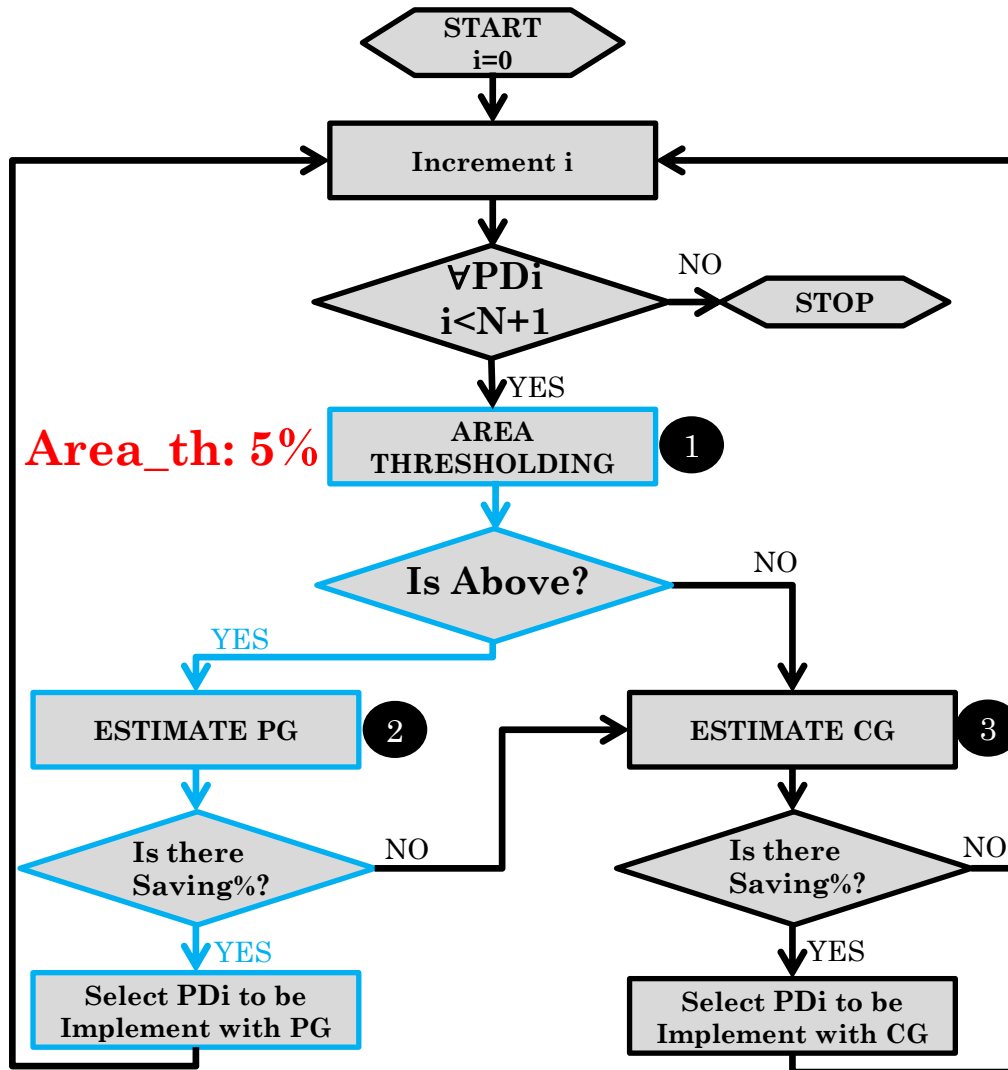
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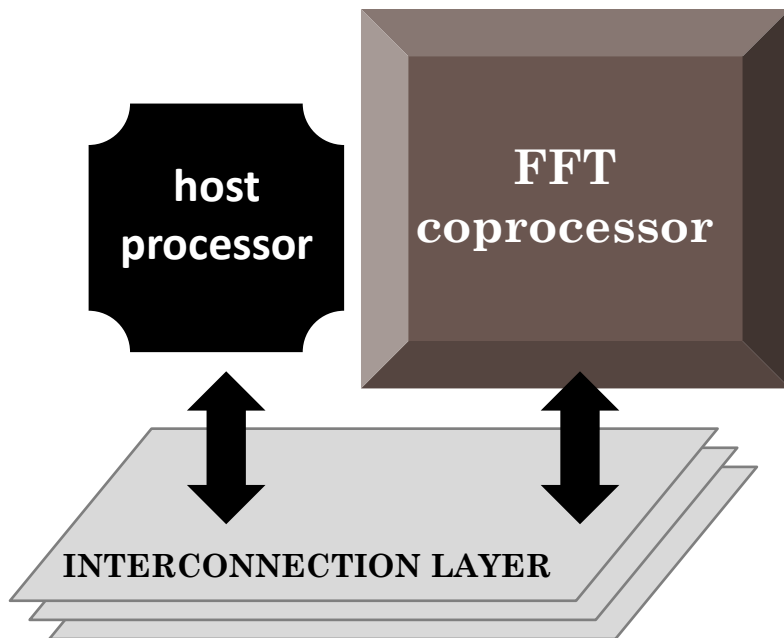


Area_th: 5%

METODOLOGY ASSESSMENT

Design Under Test: ASIC 90nm technology

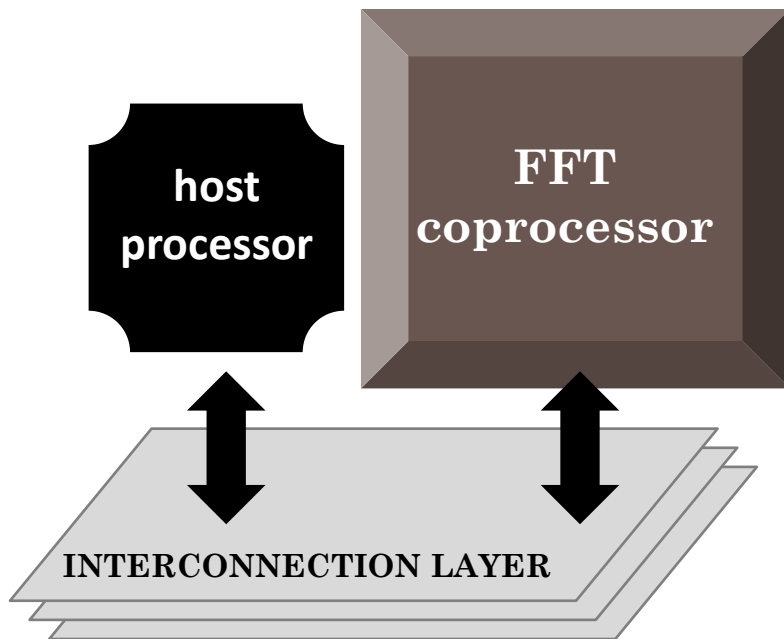
APPLICATION	# KERNEL	#LRs
FFT	4	8



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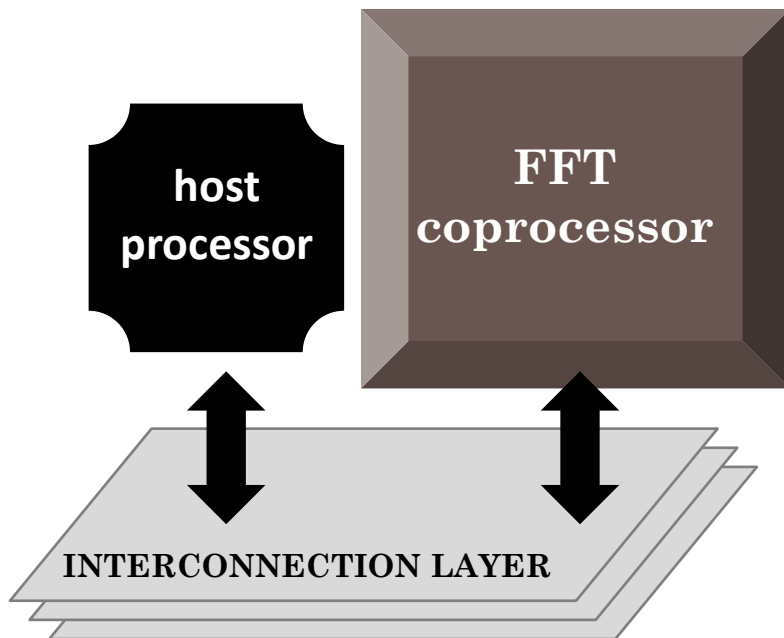


PDs	T_{iON}	#reg	Area %
PD1	33%	1024	62.44
PD2	67%	512	0.46
PD3	37%	256	15.84
PD4	4%	0	0.41
PD5	21%	0	0.25
PD6	42%	0	0.43
PD7	58%	128	7.93
PD8	96%	512	1.36

METODOLOGY ASSESSMENT

Design Under Test: ASIC 90nm technology

APPLICATION	# KERNEL	#LRs
FFT	4	8



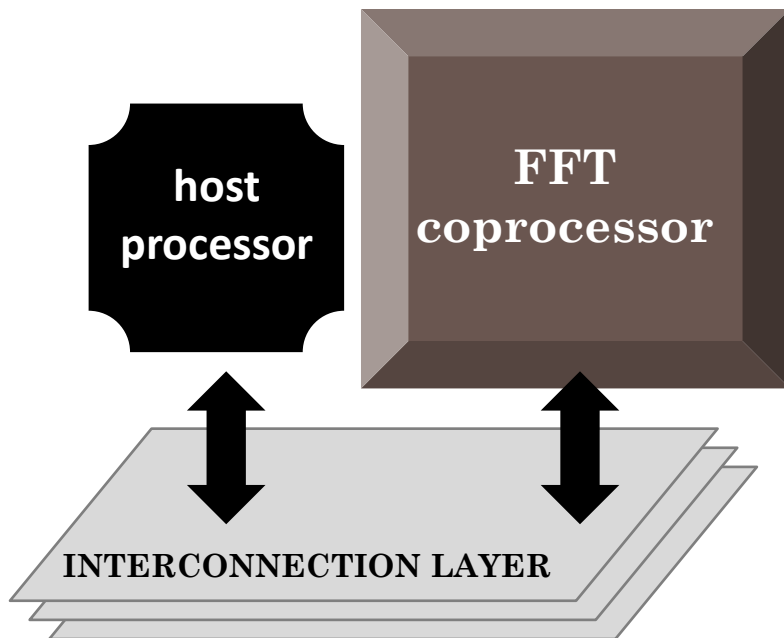
PDs	T_{iON}	#reg	Area %
PD1	33%	1024	62.44
PD2	67%	512	0.46
PD3	37%	256	15.84
PD4	4%	0	0.41
PD5	21%	0	0.25
PD6	42%	0	0.43
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Highly active

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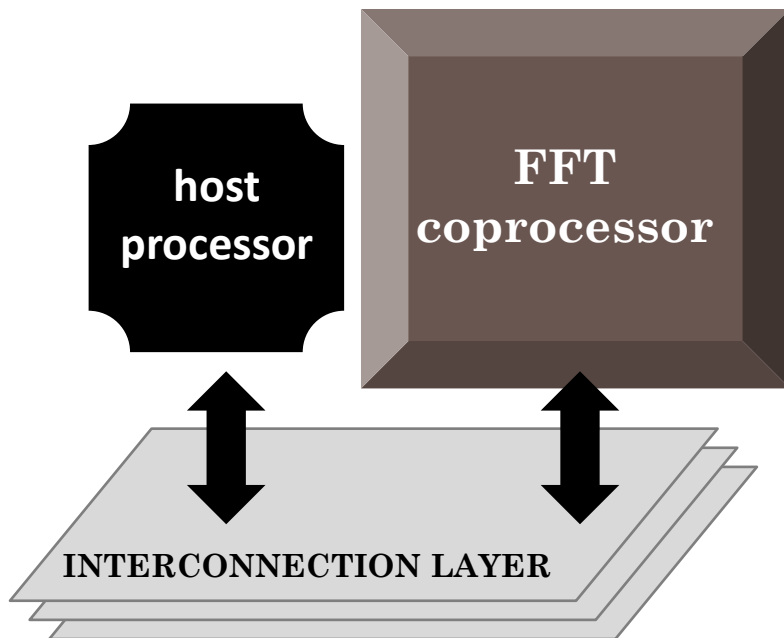
Highly active

Combinatorial

METODOLOGY ASSESSMENT

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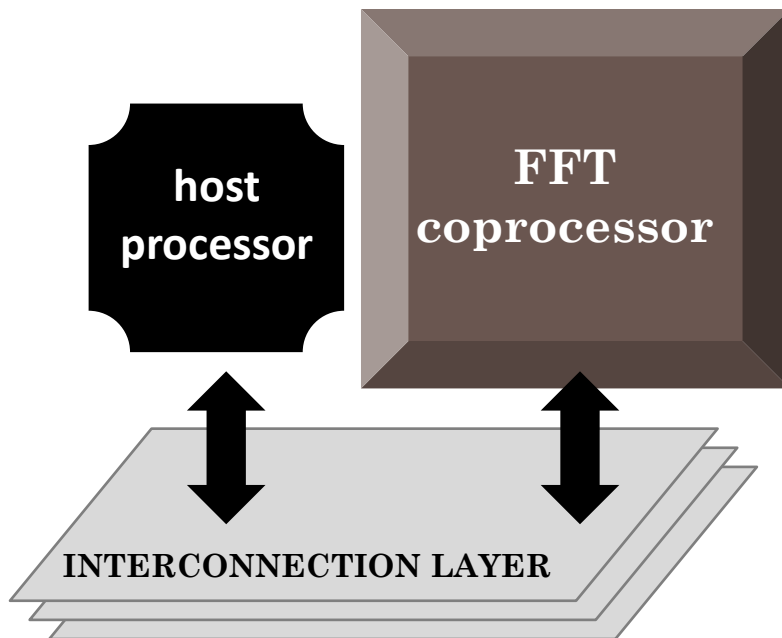
Combinatorial

Best candidate

METODOLOGY ASSESSMENT

Design Under Test: ASIC 90nm technology

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Highly active

Combinatorial

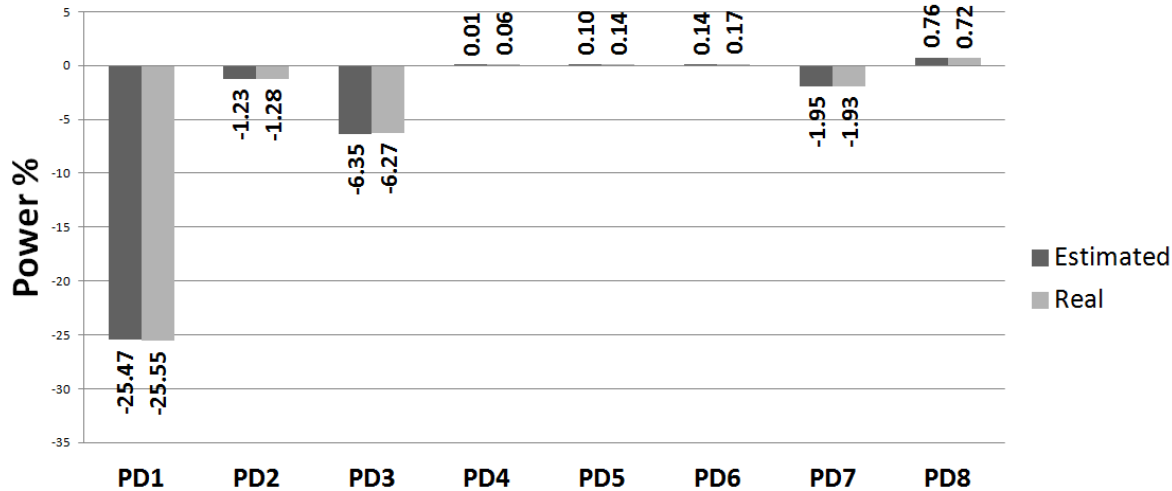
Best candidate

Small LRs

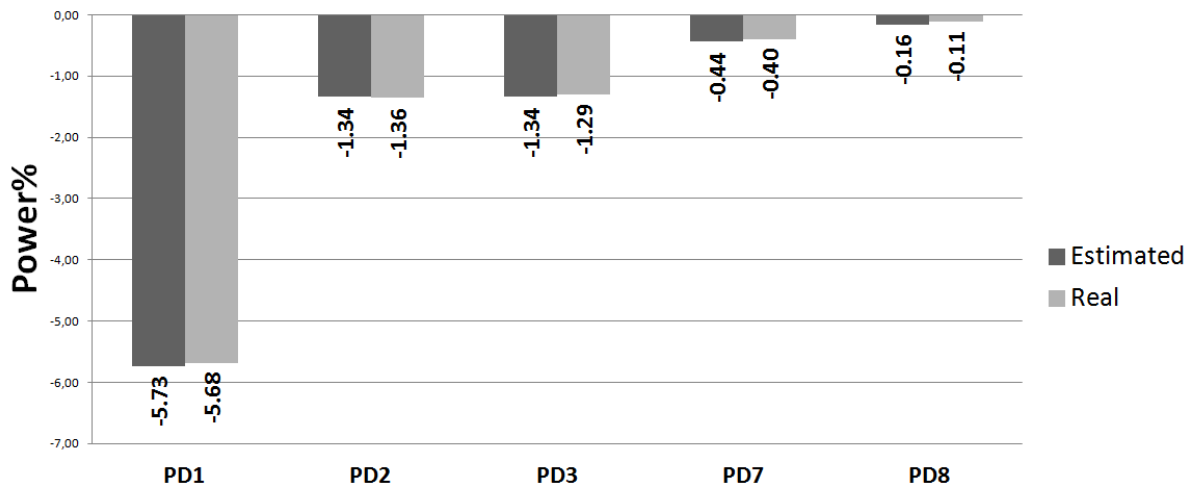
METODOLOGY ASSESSMENT

Estimated Saving

PG Power Saving



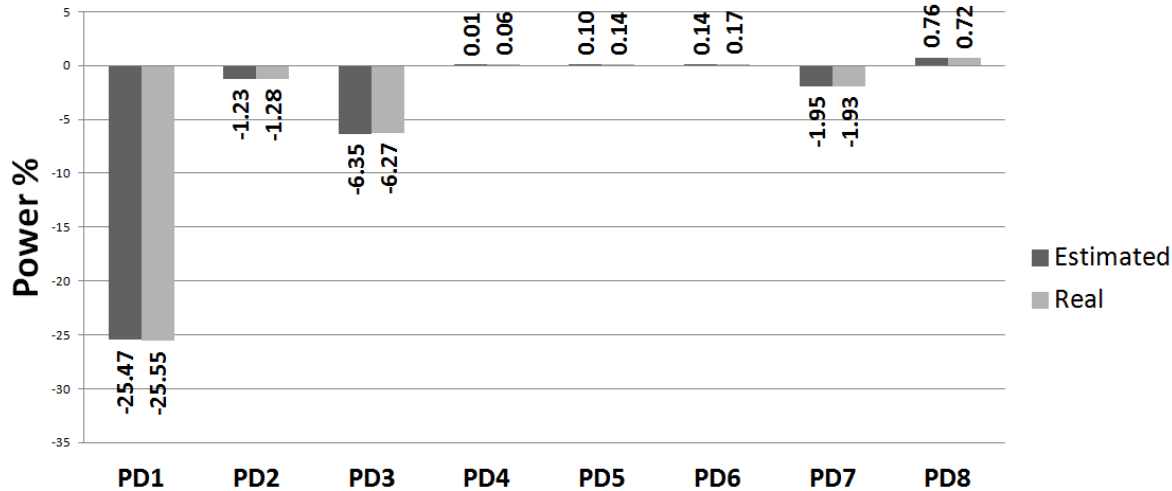
CG Power Saving



METODOLOGY ASSESSMENT

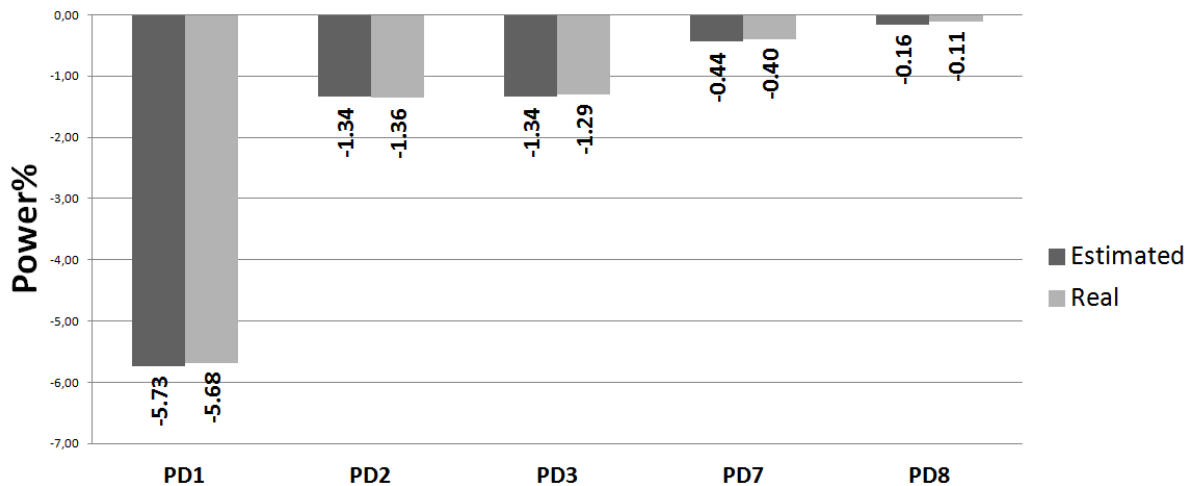
Estimated Saving

PG Power Saving



Area_th: 5% PG_1

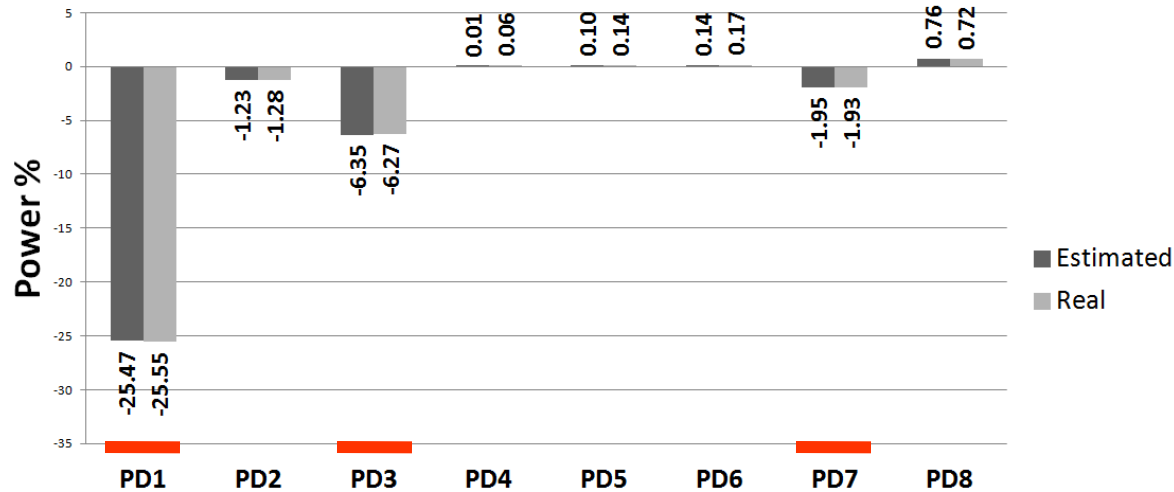
CG Power Saving



METODOLOGY ASSESSMENT

Estimated Saving

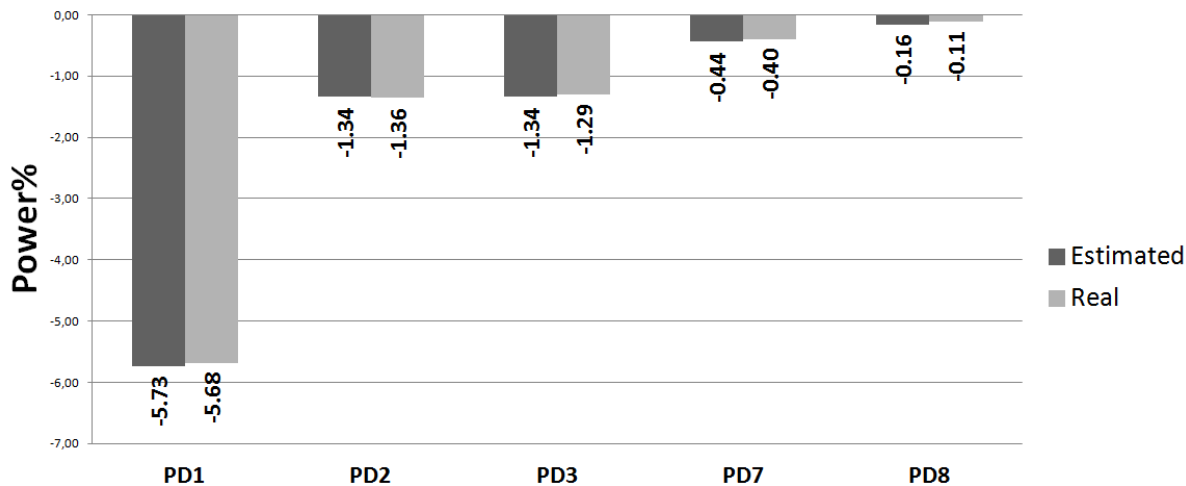
PG Power Saving



Area_th: 5% PG_1

PG PDs: PD1, PD3, PD7

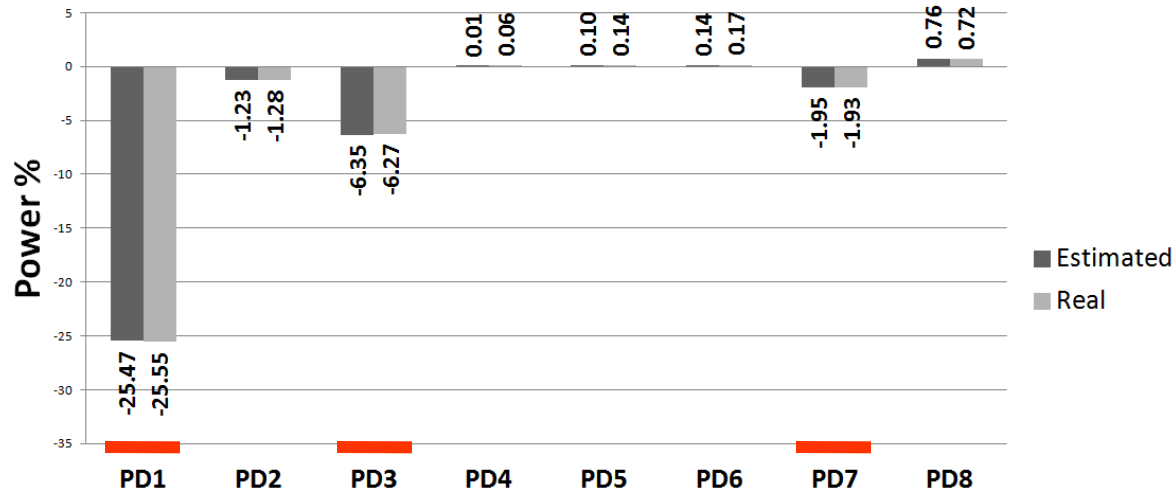
CG Power Saving



METODOLOGY ASSESSMENT

Estimated Saving

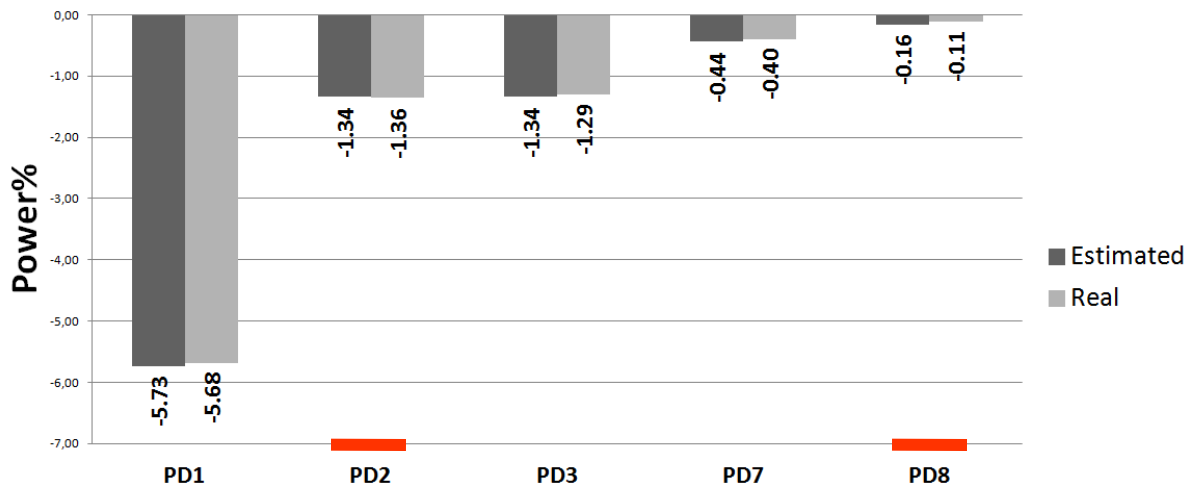
PG Power Saving



Area_th: 5% PG_1

PG PDs: PD1, PD3, PD7
CG PDs: PD2, PD8

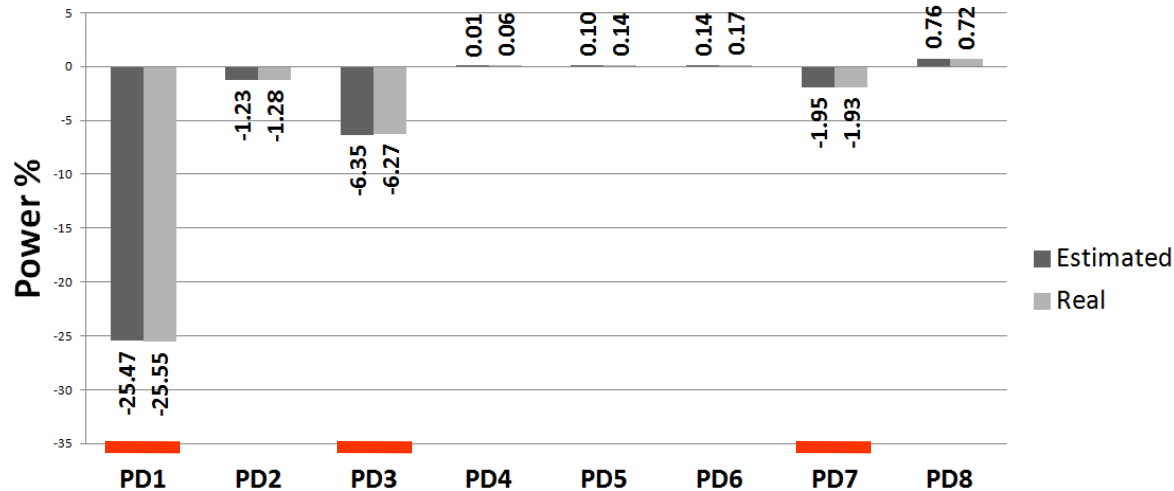
CG Power Saving



METODOLOGY ASSESSMENT

Estimated Saving

PG Power Saving

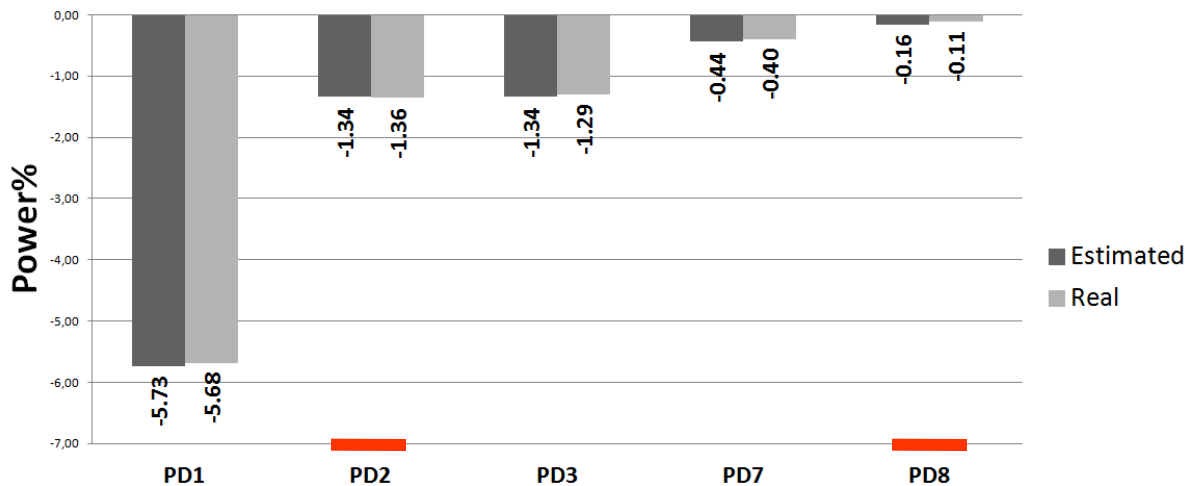


Area_th: 5% PG_1

PG PDs: PD1, PD3, PD7
CG PDs: PD2, PD8

Area_th: 10% PG_2

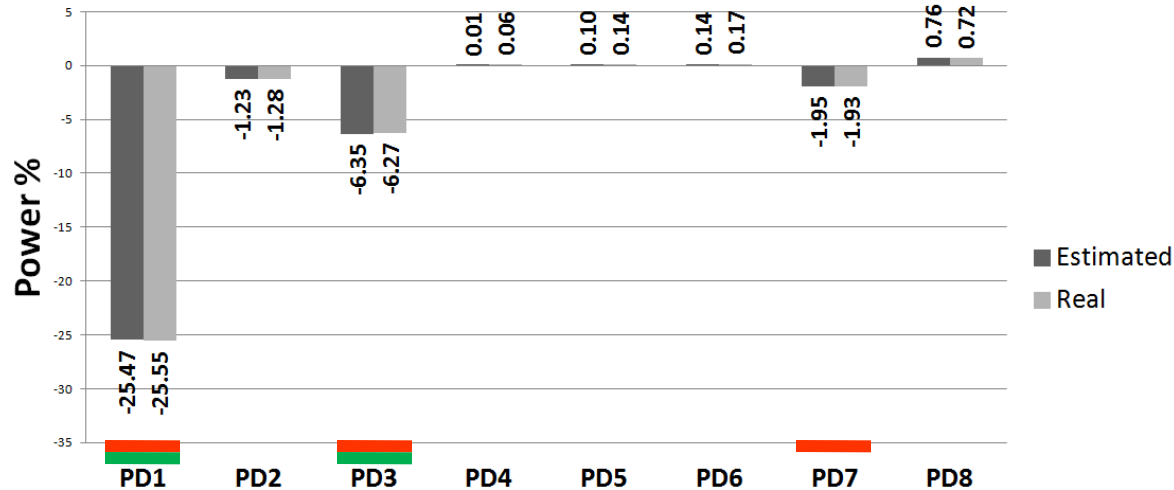
CG Power Saving



METODOLOGY ASSESSMENT

Estimated Saving

PG Power Saving



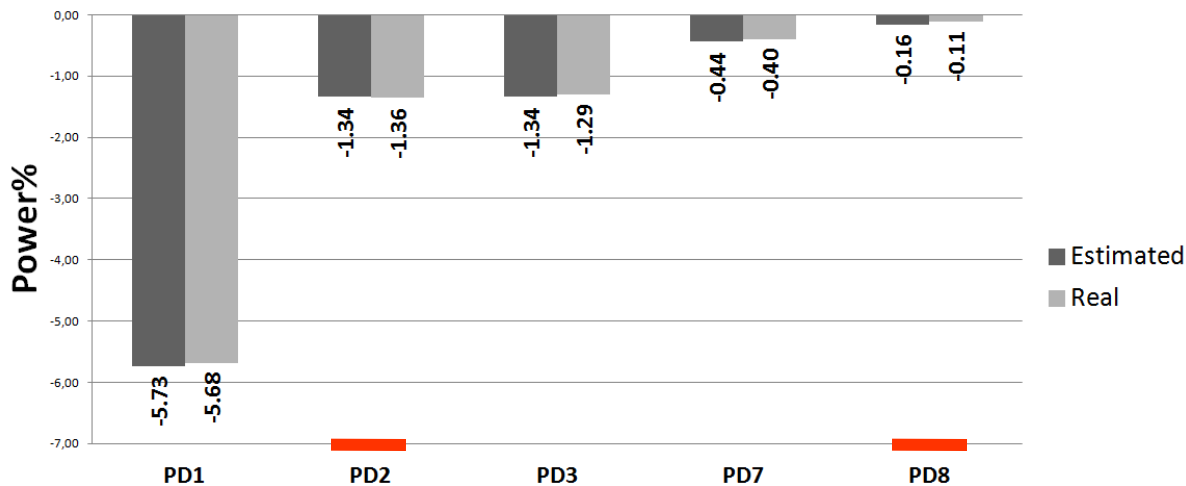
Area_th: 5% PG_1

PG PDs: PD1, PD3, PD7
CG PDs: PD2, PD8

Area_th: 10% PG_2

PG PDs: PD1, PD3

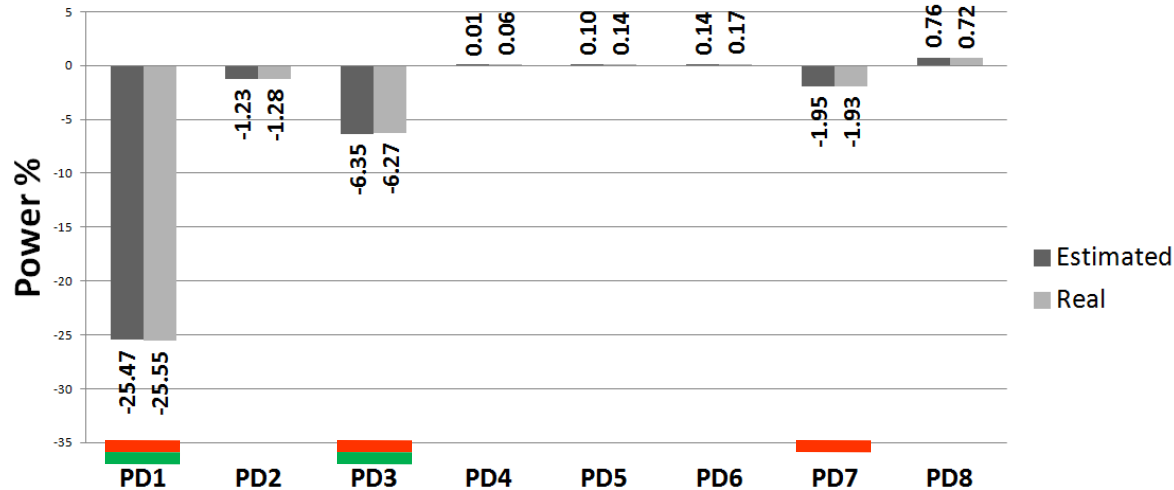
CG Power Saving



METODOLOGY ASSESSMENT

Estimated Saving

PG Power Saving



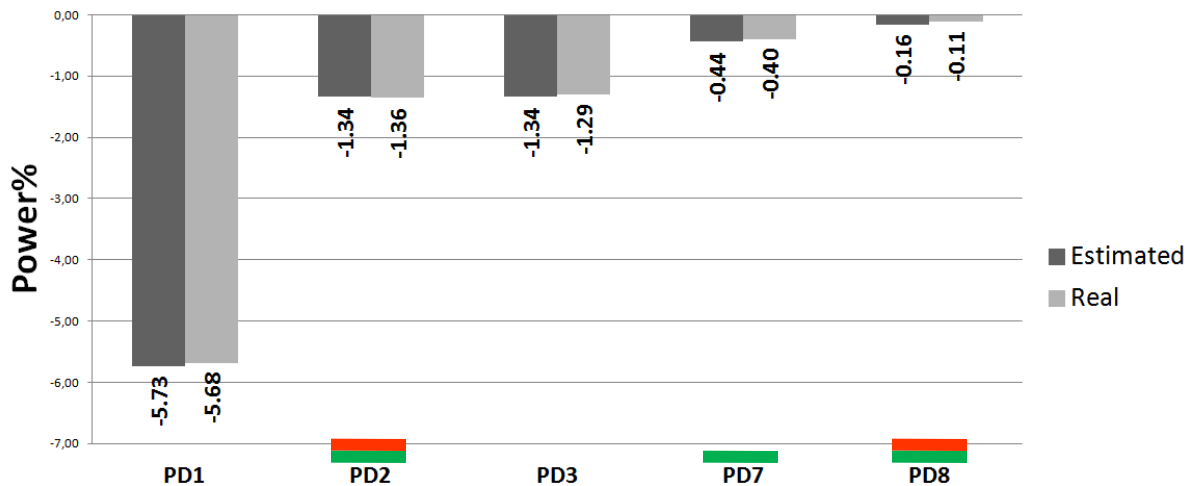
Area_th: 5% PG_1

PG PDs: PD1, PD3, PD7
CG PDs: PD2, PD8

Area_th: 10% PG_2

PG PDs: PD1, PD3
CG PDs: PD2, PD7, PD8

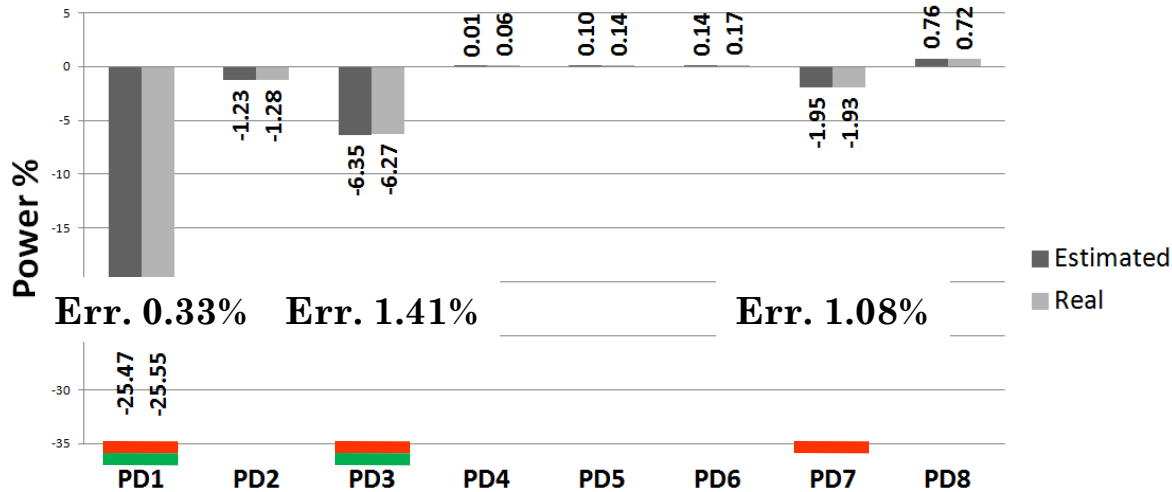
CG Power Saving



METODOLOGY ASSESSMENT

Estimated Saving

PG Power Saving



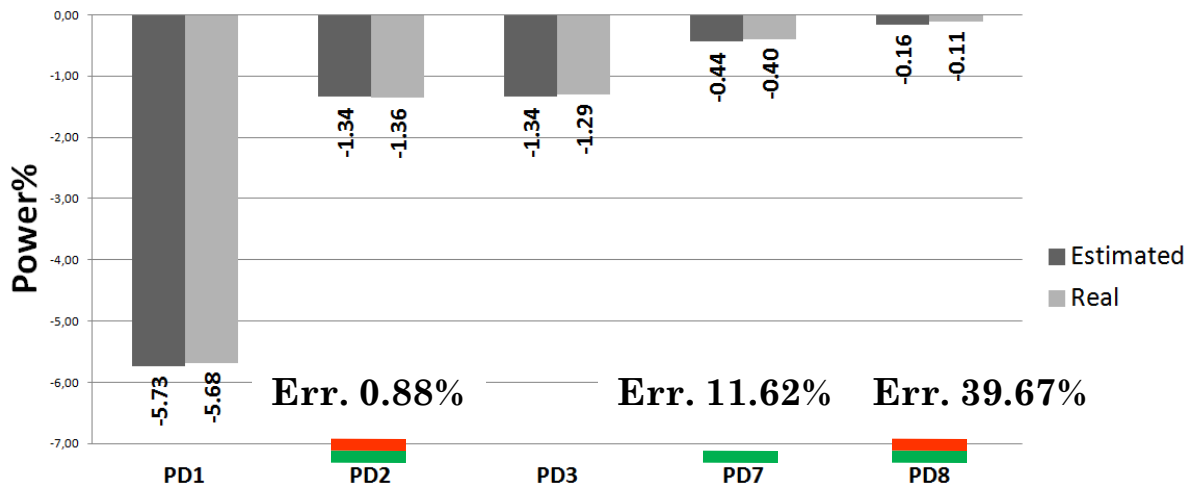
Area_th: 5% PG_1

PG PDs: PD1, PD3, PD7
CG PDs: PD2, PD8

Area_th: 10% PG_2

PG PDs: PD1, PD3
CG PDs: PD2, PD7, PD8

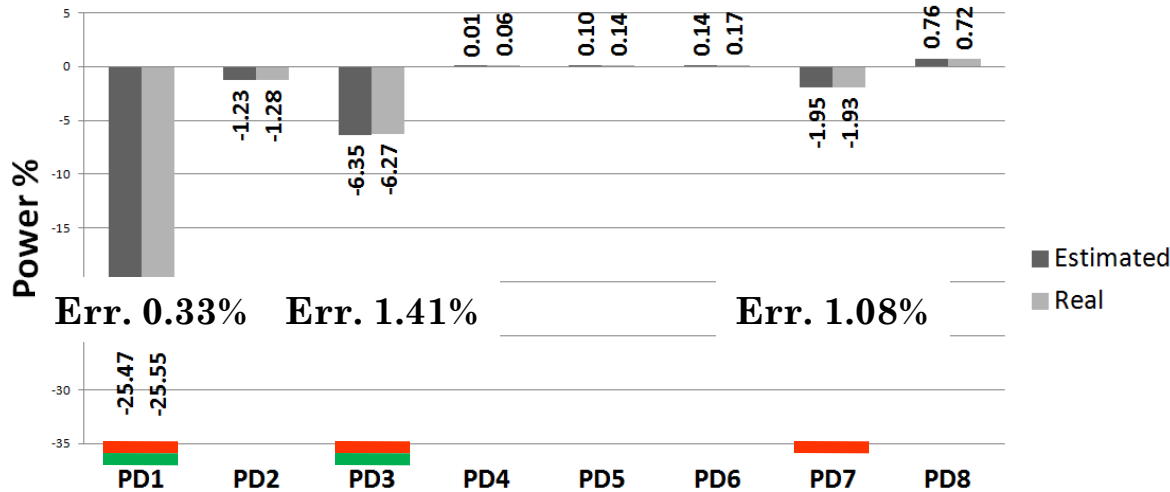
CG Power Saving



METODOLOGY ASSESSMENT

Estimated Saving

PG Power Saving



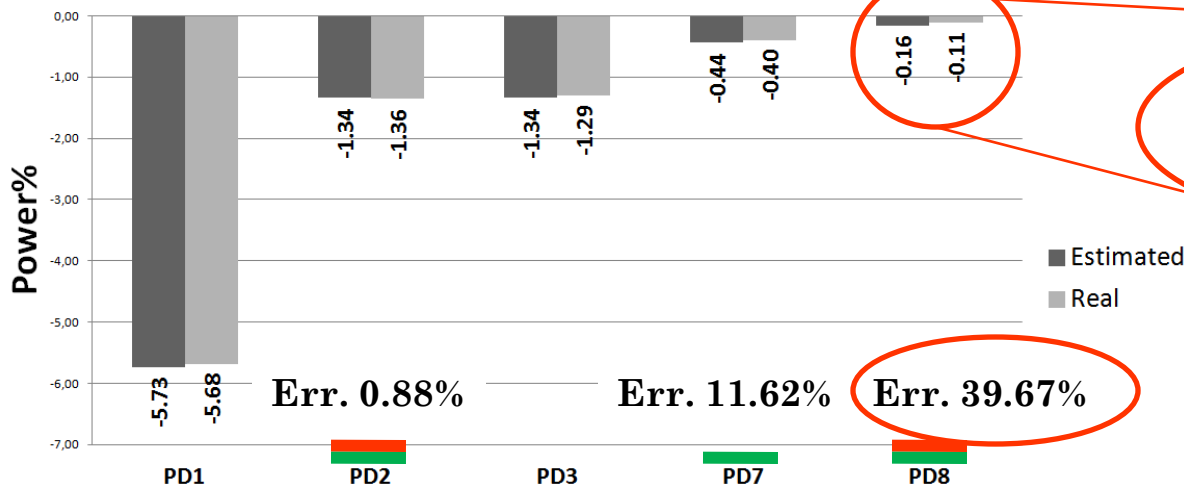
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CG Power Saving

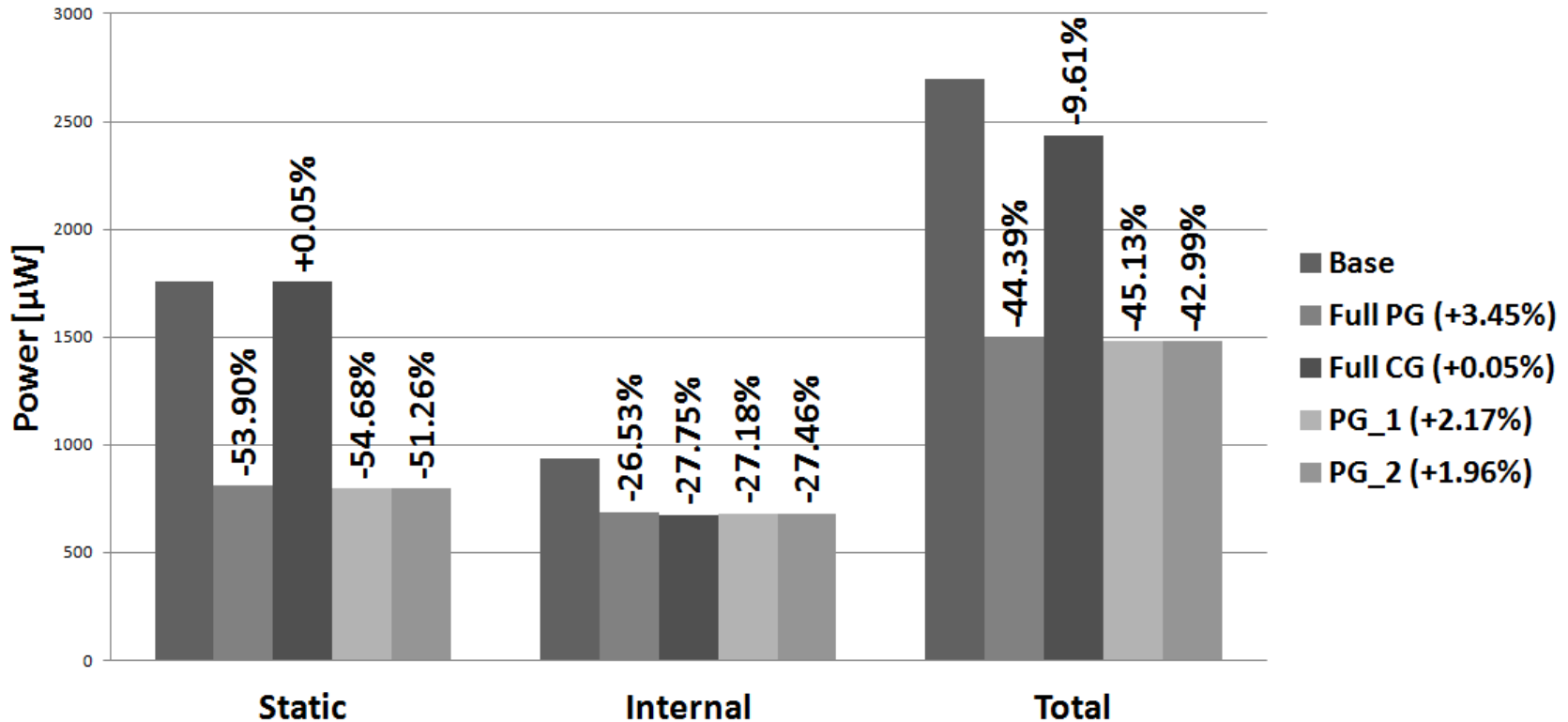


0.16% Estimated Vs
0.11% Real

METODOLOGY ASSESSMENT

Designs Comparison

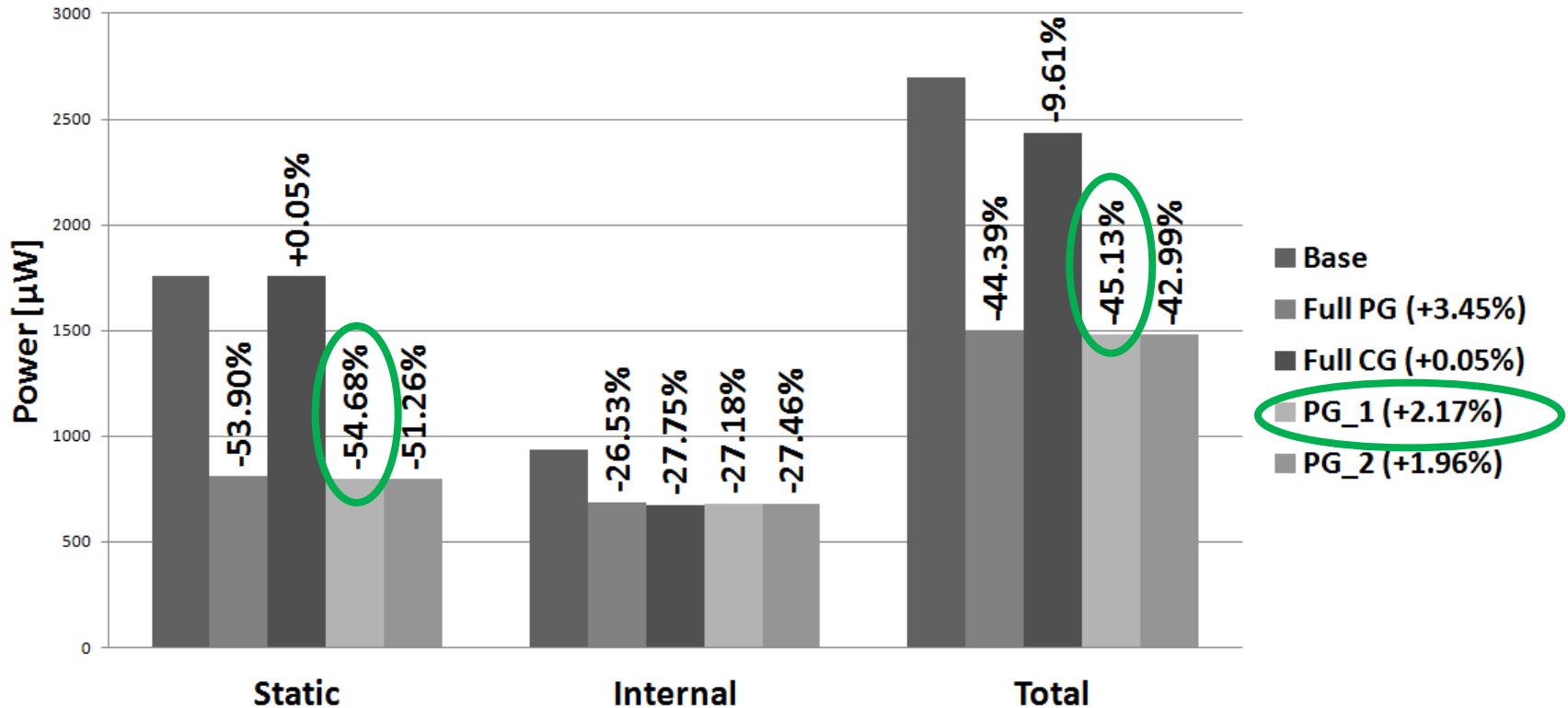
Power Consumption



METODOLOGY ASSESSMENT

Designs Comparison

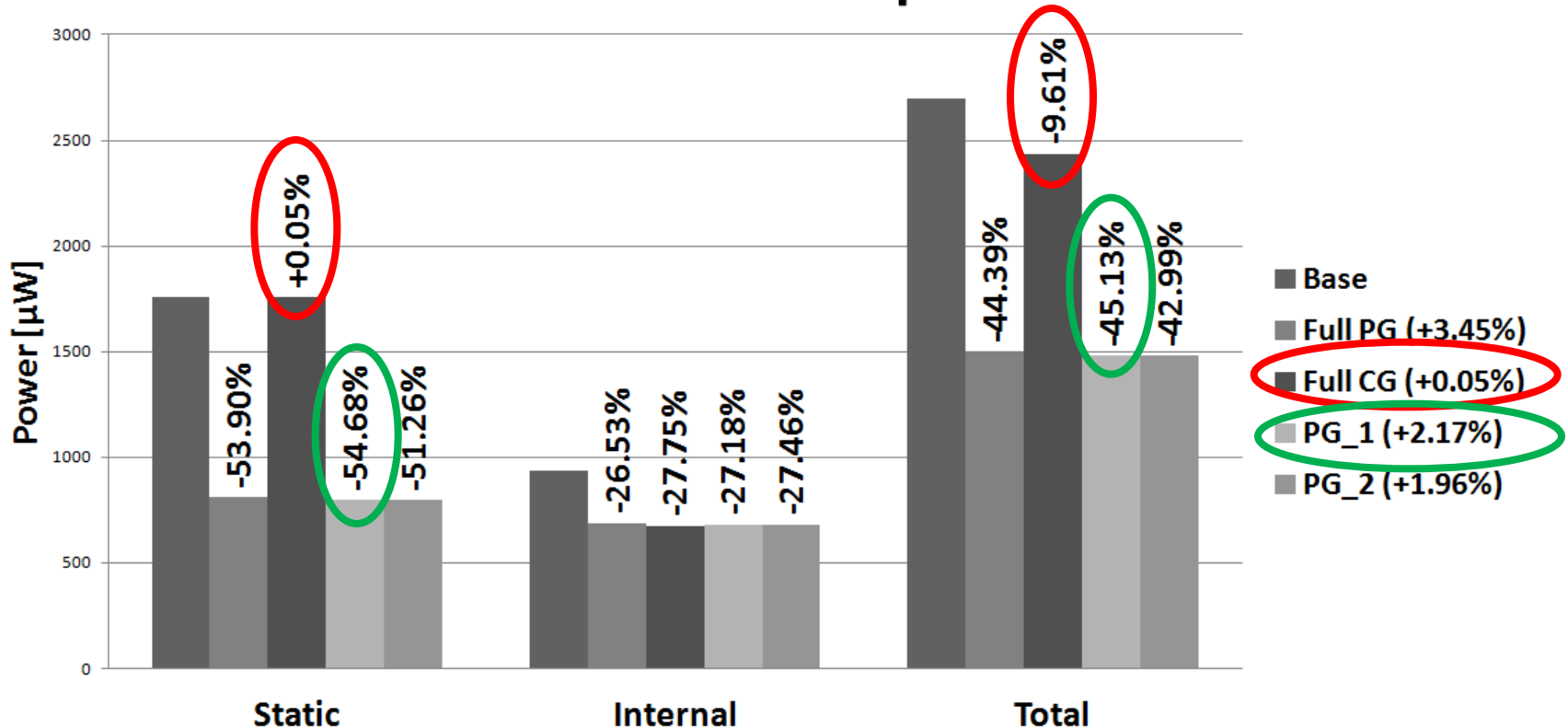
Power Consumption



METODOLOGY ASSESSMENT

Designs Comparison

Power Consumption



CONCLUSIONS

Advantages of the proposed approach

- Given a CGR design with **n kernel** and **k LR**s

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Advantages of the proposed approach

- Given a CGR design with **n kernel** and **k LRs**
- The proposed approach requires uniquely the analysis of the baseline CGR design:
 - one synthesis
 - **n simulations** (one foreach kernel)

CONCLUSIONS

Advantages of the proposed approach

- Given a CGR design with **n kernel** and **k LRs**
- The proposed approach requires uniquely the analysis of the baseline CGR design:
 - one synthesis
 - **n simulations** (one for each kernel)
- Otherwise:
 - $(2*k+1)$ (one PG and one CG for each LR + one of Base the design)
 - $(2*k+1)*n$ **simulation** (n simulation for each design)

ACKNOWLEDGEMENTS

- The research leading to these results has received funding from:
 - the Region of Sardinia L.R.7/2007 under grant agreement CRP-18324 [RPCT Project].
 - the Region of Sardinia, Young Researchers Grant, POR Sardegna FSE 2007-2013, L.R.7/2007 “Promotion of the scientific research and technological innovation in Sardinia”





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