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Power and Clock Gating Modelling in Coarse Grained Reconfigurable Systems

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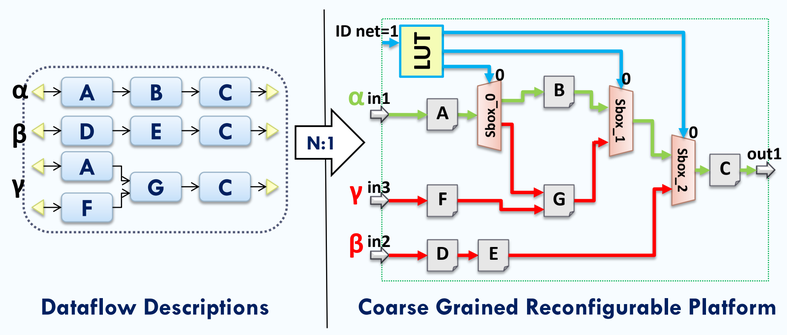
Abstract

In the context of **Coarse Grained Reconfigurable** systems we propose a way to model power and clock gating costs based on the parameters of the baseline CGR system. The proposed flow guides designers towards optimal implementations, saving designer effort and time. The model is assessed by adopting a reconfigurable core for FFT targeting an **ASIC 90 nm technology**.

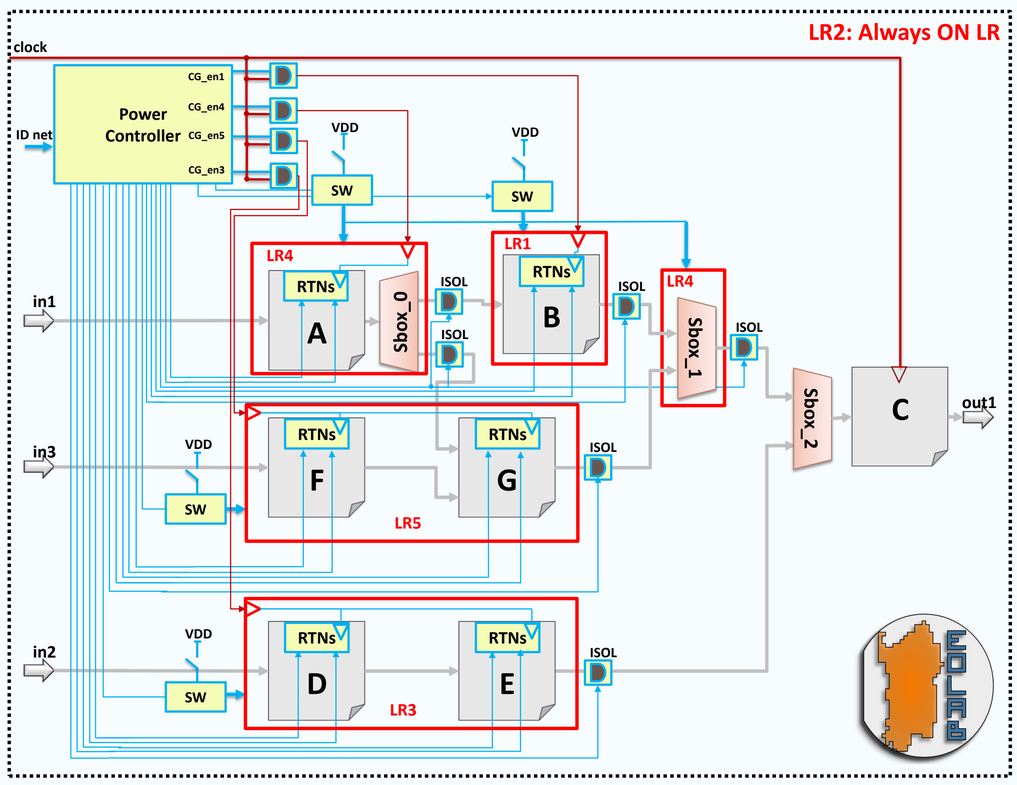
Coarse Grained Reconfigurable (CGR) Systems

CGR systems offer high-performance and flexibility. However their efficient design is complex and they may require large power consumption due to the fact that not all the resources are involved in the computation.



Dataflow Descriptions — Coarse Grained Reconfigurable Platform

To save both dynamic and static power, **Clock Gating** (**CG**) and **Power Gating** (**PG**) can be respectively used. While all the main commercial synthesizers apply automatic CG, they do not provide automatic PG methodologies.



Multi-Dataflow Composer Tool

The **Multi-Dataflow Composer** (**MDC**) tool provides automatic datapath merging starting from different Dataflow Descriptions (DDs). It identifies the minimum set of Functional Units (FUs) always active together, called **Logic Regions** (**LRs**), and **blindly** applies to all of them:

CG: by inserting a CG cell for each LR.

PG: by inserting all the necessary PG logic.

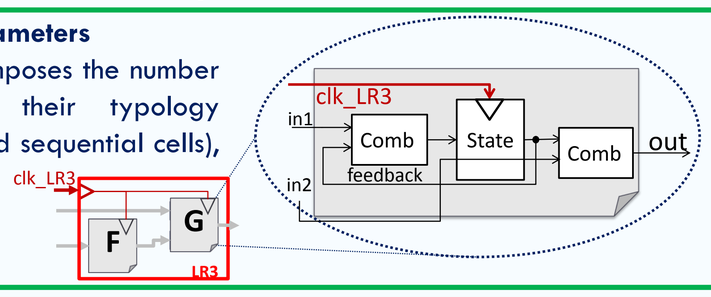
- ***sleep transistors*** to switch on/off the power supply.
- ***isolation cells*** to avoid the transmission of spurious signals in input to the normally-on cells.
- ***state retention*** logic to maintain the internal state of the gated region.

http://sites.unica.it/rpct/

Parameters Specification

Architectural parameters

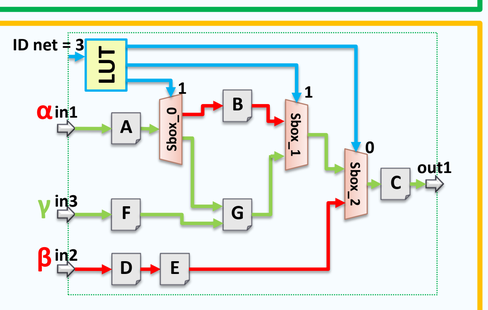
LRs composition imposes the number of gates and their typology (combinatorial and sequential cells), determining the region basic consumption.



Functional parameters

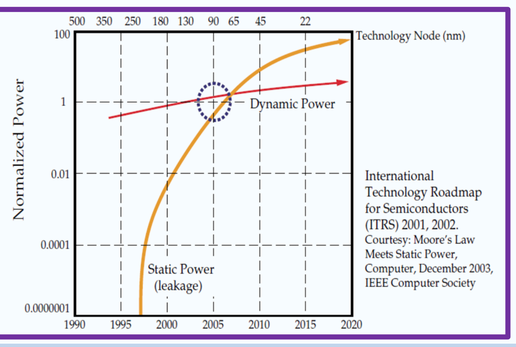
Input data impose the behaviour of the reconfigurable design and the activation time of LRs.

ID_net	Net	Sbox_0	Sbox_1	Sbox_2	LRs
1	α	0	0	0	LR1, LR2, LR4
2	β	X	X	1	LR2, LR3
3	γ	1	1	0	LR2, LR4, LR5



Technological parameters

The targeted technology decides the ratio between the two power consumption terms. As transistors get smaller the contribution of the static contribute gets larger and not negligible anymore.



Power Estimation Model.

P_{ON}(LRi): power consumption **inside** considered region.
Ext_Over(LRi): power consumption due to the additional logic inserted **outside** the region.

Power Gating model.

$$P(LR_i) = P_{ON}(LR_i) + Ext\_Over(LR_i) =$$

$$= \sum_{actors \in LR_i} [P(cmb) + P(RC)*\#rtn + P(reg)*(\#reg - \#rtn)/\#reg]*T_{iON} +$$

$$+ [P(ISO_{ON})*\#iso*T_{iON} + P(ISO_{OFF})*\#iso*T_{iOFF}] +$$

$$+ [P(Contr_{ON})*T_{iON} + P(Contr_{OFF})*T_{iOFF}] +$$

$$+ [P(CG_{ON})*T_{iON} + P(CG_{OFF})*T_{iOFF}]$$

Clock Gating model.

$$P(LR_i) = P_{ON}(LR_i) + Ext\_Over(LR_i) =$$

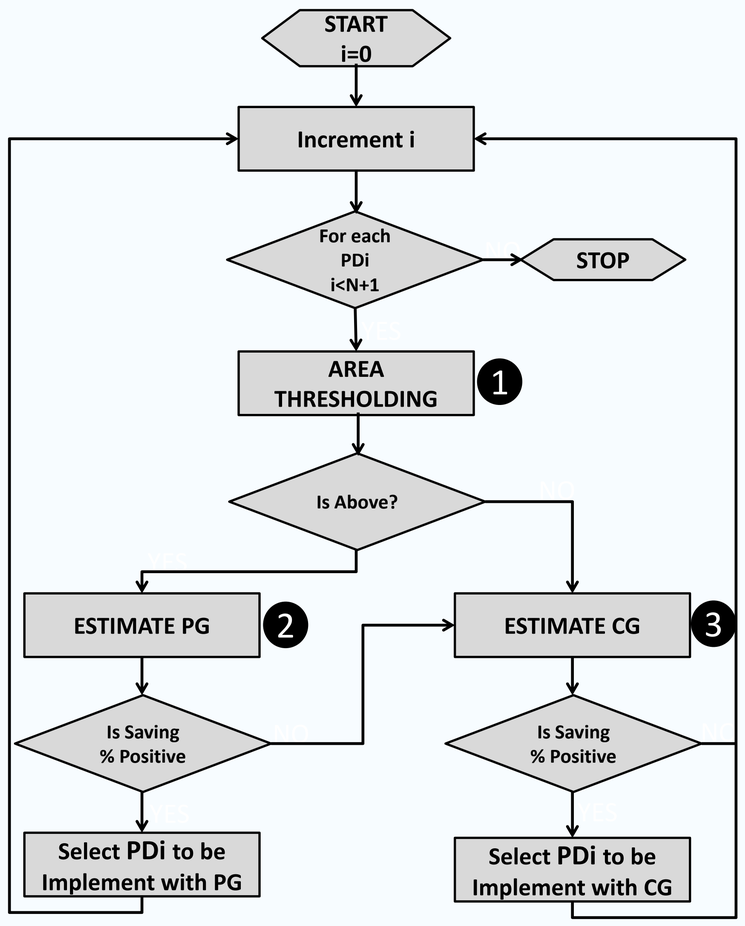
$$= \sum_{actors \in LR_i} [P(cmb) + P(reg)*T_{iON}] +$$

$$+ [P(CG_{ON})*T_{iON} + P(CG_{OFF})*T_{iOFF}]$$

Term not present in the static estimation model of clock gated designs!

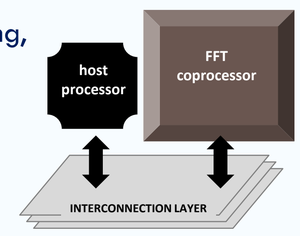
Standard Cost	Overhead
Combinational Logic	Retention Cells
	Isolation Cells
Sequential Logic	Power Controller
	Clock Gating Cells

Power Estimation Flow



Methodology Assessment on ASIC

A CGR coprocessor for image processing, involving eight computational kernels, has been assembled with MDC.

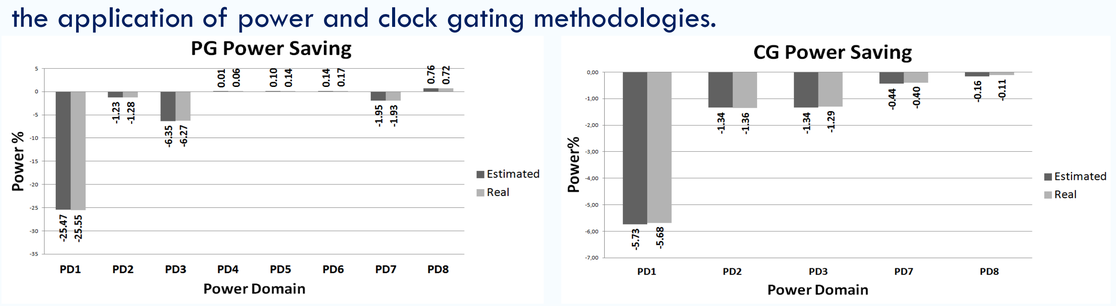


APPLICATION	# KERNEL	#LRs
FFT	4	8

LRs	Ti_{ON}	#reg	Area%	#rtn	#iso(e)	#riso(r)
LR1	0.33	1024	62.44	1024	1024	1024
LR2	0.67	512	0.46	3	1112	1032
LR3	0.37	256	15.84	256	512	512
LR4	0.04	0	0.41	0	2324	2306
LR5	0.21	0	0.25	0	1948	1926
LR6	0.42	0	0.43	0	1756	1740
LR7	0.58	128	7.93	128	256	256
LR8	0.96	512	1.36	512	5259	4934

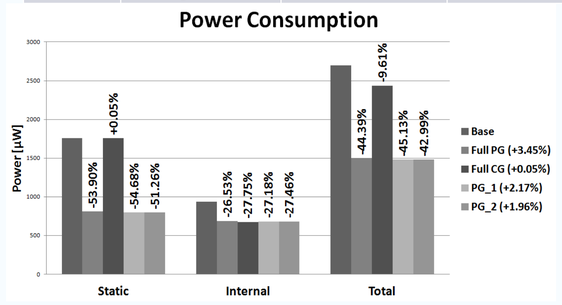
Ti_{ON}: percentage activation time.
#reg: number of sequential elements.
Area%: LR's percentage area wrt total area.
#rtn: number of retention cells.
#iso(e): estimated number of isolation cells.
#iso(r): real number of isolation cells.

Histograms report, for each LR, the estimated and real power consumption variation after the application of power and clock gating methodologies.



To assess the efficiency of the proposed model we compare different designs:

Base	PG_full	CG_full	PG_1: area_th 5%		PG_2_ area_th 10%	
All LRs ON	All LRs power gated	All LRs clock gated	PG LRs: 1, 3, 7	CG LRs: 2, 8	PG LRs: 1, 3	CG LRs: 2, 8,7



Histograms report results for the different designs. PG_1 has the best tradeoff between power saving and area overhead. Full_CG is saves larger dynamic power but has less benefit in terms of total power consumption.

Advantage of the Proposed Approach

The proposed approach requires uniquely one synthesis and n different simulations. Without the proposed models, the identification of the most convenient PDs to be switched off: 1) to implement one power gated and one clock gated design for each PD, and 2) to compare them with respect to the baseline CGR.