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POWER MODELLING FOR SAVING STRATEGIES IN COARSE GRAINED RECONFIGURABLE SYSTEMS

Tiziana Fanni, Carlo Sau, Paolo Meloni and Luigi Raffo
University of Cagliari - Dept. of Electrical and Electronics Eng.
(tiziana.fanni, carlo.sau, paolo.meloni, luigi)@diee.unica.it

Francesca Palumbo
University of Sassari - PolComIng Information Engineering Unit
fpalumbo@uniss.it

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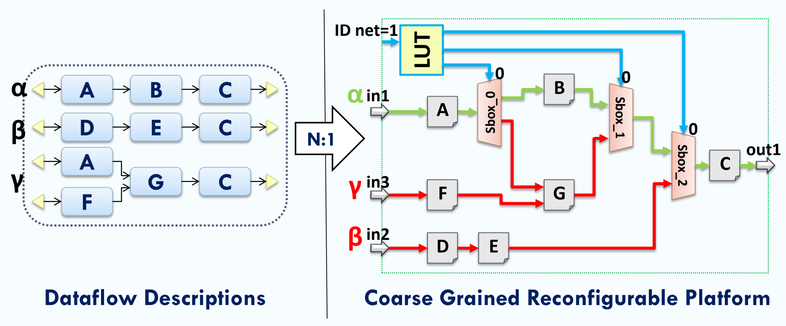
Abstract

In the context of coarse grained reconfigurable systems we present a **power estimation model** to guide the designer in deciding which part of the design may benefit from the application of a **power gating** technique. The model is assessed by adopting a reconfigurable core for image processing targeting an **ASIC 90 nm technology**.

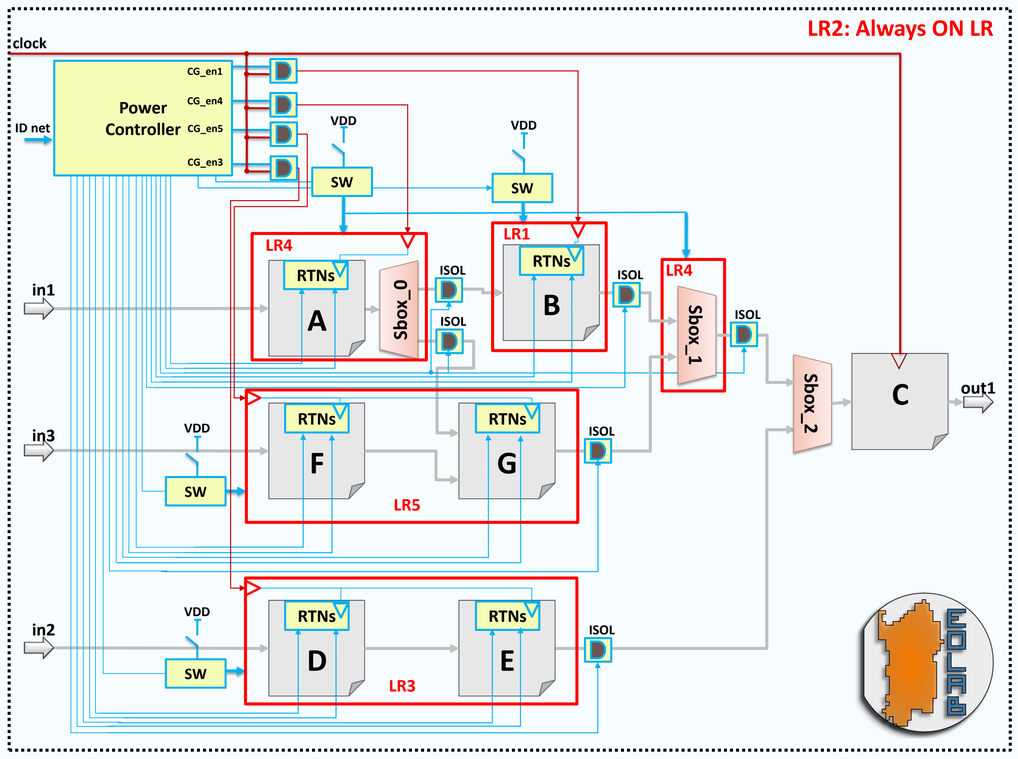
Coarse Grained Reconfigurable (CGR) Systems

CGR systems offer high-performance and flexibility. However their efficient design is complex and they may require large power consumption due to the fact that not all the resources are involved in the computation.



Dataflow Descriptions — Coarse Grained Reconfigurable Platform

To save both dynamic and static power, **Clock Gating** (**CG**) and **Power Gating** (**PG**) can be respectively used. While all the main commercial synthesizers apply automatic CG, they do not provide automatic PG methodologies.



Multi-Dataflow Composer Tool

The **Multi-Dataflow Composer** (**MDC**) tool provides automatic datapath merging starting from different Dataflow Descriptions (DDs). It identifies the minimum set of Functional Units (Fus) always active together, called **Logic Regions** (**LRs**), and **blindly** applies to all of them:

CG: by inserting a CG cell for each LR.

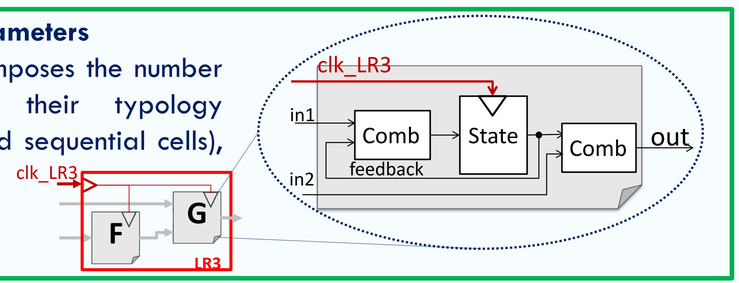
PG: by inserting all the necessary PG logic.

- ***sleep transistors*** to switch on/off the power supply.
- ***isolation cells*** to avoid the transmission of spurious signals in input to the normally-on cells.
- ***state retention*** logic to maintain the internal state of the gated region.

Parameters Specification

Architectural parameters

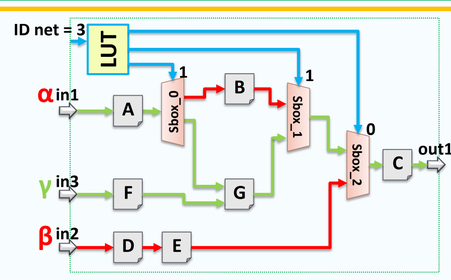
LRs composition imposes the number of gates and their typology (combinatorial and sequential cells), determining the region basic consumption.



Functional parameters

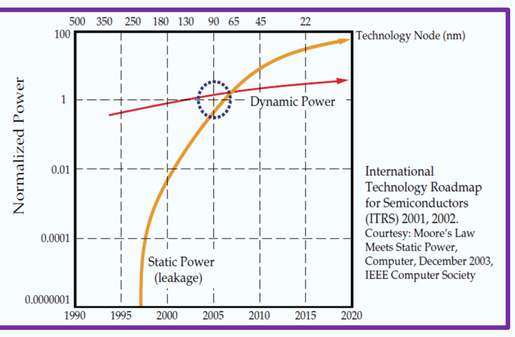
Input data impose the behaviour of the reconfigurable design and the activation time of LRs.

ID_net	Net	Sbox_0	Sbox_1	Sbox_2	LRs
1	α	0	0	0	LR1, LR2, LR4
2	β	X	X	1	LR2, LR3
3	γ	1	1	0	LR2, LR4, LR5



Technological parameters

The targeted technology decides the ratio between the two power consumption terms. As transistors get smaller the contribution of the static contribute gets larger and not negligible anymore.



Static Power Estimation Model.

$$P_{lkg}(LR_i) = P_{lkgON}(LR_i) + ISO_{overhead}(LR_i) =$$

$P_{lkg\ ON}(LRi)$: static power consumption of the considered region when it is activated

$ISO_{overhead}(LRi)$: static power consumption due to the overhead of inserting the isolation cells within the neighbouring LRs.

$$= \sum_{actors \in LR_i} [P_{lkg}(cmb) + P_{lkg}(RC)*\#reg]*T_{iON} +$$

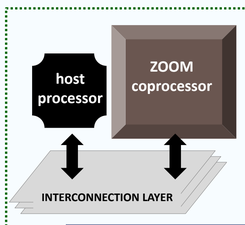
$$+ [P_{lkg}(ISO_{ON})*\#iso*T_{iON} + P_{lkg}(ISO_{ON})*\#iso*(1-T_{iON})]$$

P_{lkg} ON: summation over all the actors within the LR, weighted by the LR percentage of activation time TiON, of the:

- leakage power due to the combinatorial logic, **$P_{lkg}(comb)$**;
- leakage power due to the sequential cells, derived as the number of them (#reg) multiplied by the average consumption of a retention cell (**$P_{lkg}(RC)$**) whereby they are replaced;

$ISO_{overhead}$: summation of the number of isolation cells (**#iso**) within the LR multiplied by:
the average consumption of an active isolation cell (**$P_{lkg}(ISO_{ON})$**) multiplied by the activation time **Ti_{ON}**;
the average consumption of an inactive isolation cell (**$P_{lkg}(ISO_{OFF})$**) multiplied by the inactive time (**1- Ti_{ON}**).

Methodology Assessment



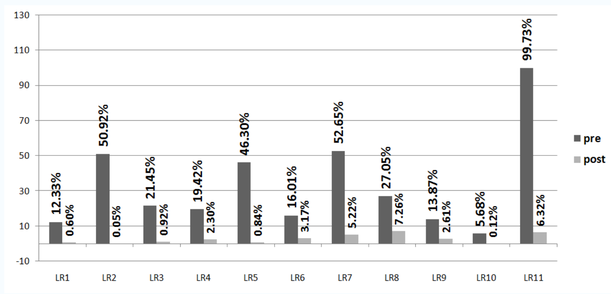
A CGR coprocessor for image processing, involving seven high computational kernels, has been assembled with MDC.

APPLICATION	# KERNEL	#ACTORS	# SBOXES	#LRs
zoom	7	33	51	11

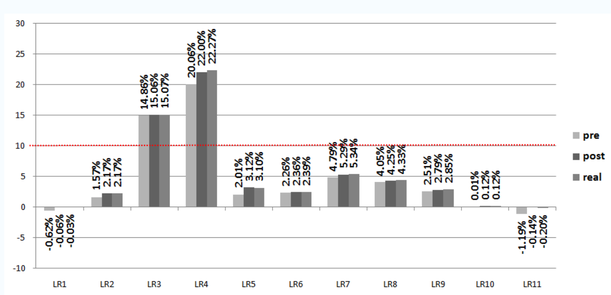
LRs	Ti_{ON}	#iso	#reg	#real_iso	#real_reg
LR1	46.2	465	148	355 (30.99)	140 (5.71)
LR2	18.9	230	137	78 (194.87)	122 (12.30)
LR3	3.3	153	281	101 (51.49)	233 (20.60)
LR4	21.7	385	1420	185 (93.51)	1040 (36.5)
LR5	17.1	505	239	355 (42.25)	30 (696.67)
LR6	11.8	106	110	81 (30.86)	100 (10.00)
LR7	8.5	208	252	70 (197.14)	283 (7.14)
LR8	30.2	153	218	100 (53.00)	206 (5.83)
LR9	24.5	153	236	101 (51.49)	213 (10.80)
LR10	46.8	100	74	83 (17.65)	70 (5.71)
LR11	27.7	303	69	90 (283.89)	25 (176.00)

Ti_{ON}: percentage activation time.
#iso: estimated number of isolation cells.
#reg: number of sequential elements.
#real_iso: real number of instantiated isolation cells.
#real_reg: number of sequential elements replaced by retention cells.
(Estimation errors are give in brackets.)

Histogram report, for each LR, the percentage error of the estimated static power consumption with respect to measured (extracted from the post-synthesis reports) one.



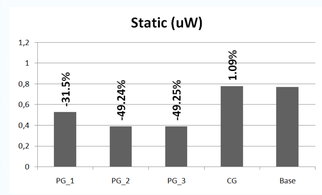
Estimated percentage saving/overhead that the implementation of PG over each LR would imply. LR3 and LR4 switching off determine the highest power saving (more than 10%).

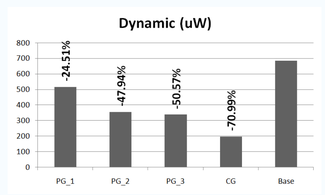


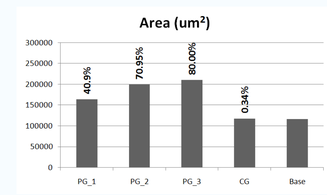
To assess the efficiency of the proposed model we compared different designs:

PG_1	PG_2	PG_3
Off LRs: 3, 4	Off LRs: 2, 3, 4, 5, 6, 7, 8, 9	Off LRs: All

Histograms report results for the three designs where PG is applied (PG_n), a design where CG is applied, and a design without power saving (Base). PG_1 has the best tradeoff between power saving and area overhead. As expected, CG is capable of saving larger dynamic power and presents quite no area overhead, but it is not capable of proving any benefit in terms of static power consumption.







Conclusions and PhD plan

The presented power estimation model allows us to predict when a LR benefits from the application of PG techniques.
As a future PhD plan, it is necessary to:

- **develop dynamic model**: a similar study about the dynamic power consumption should be executed, in order to derive a dynamic power estimation model.
- **asses technology**: different technologies need to be explored, to check whether the proposed model need to be adjusted.
- **automate strategy**: integration of the proposed parameter analysis and estimation model within the MDC automatic flow.