2014 IEEE International Workshop on **Si**gnal **P**rocessing **S**ystems
October 20 – 22 2014, Belfast, UK
SIPS 2014

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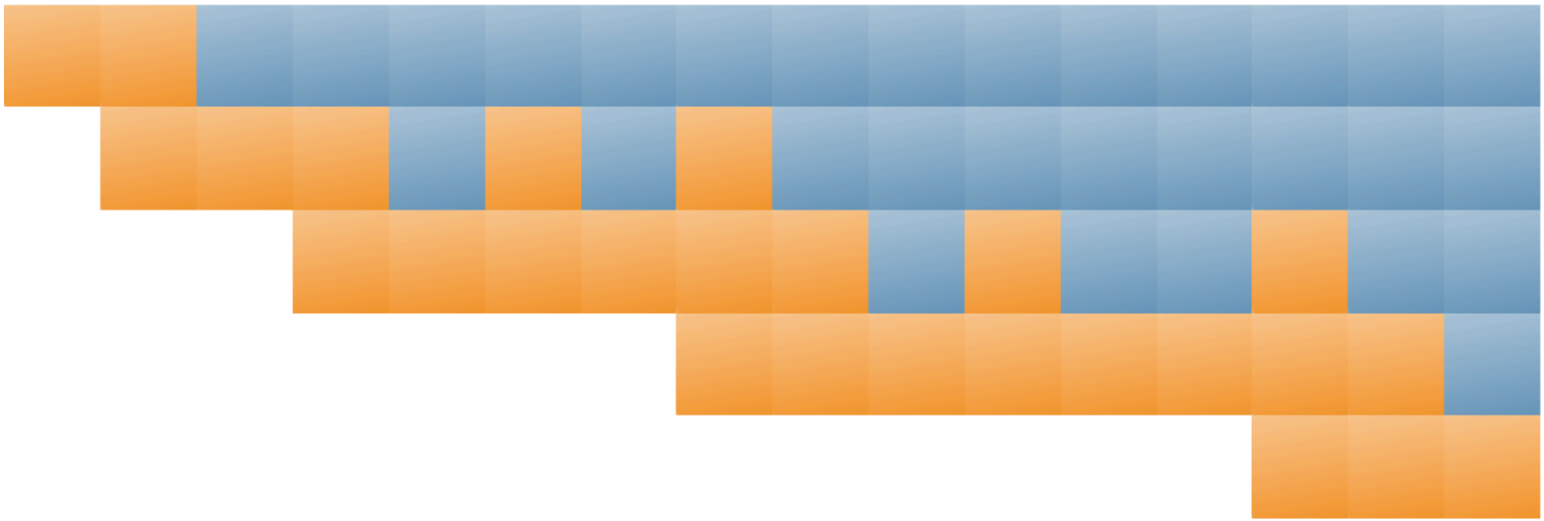
Università degli Studi di Sassari
PolComIng – Information Engineering Unit

Power-Awareness in Coarse-Grained Reconfigurable Designs: a Dataflow Based Strategy



OUTLINE

- Introduction
  - Problem statement
  - Background
  - The power issue
- Automatic Power-Awareness Strategies
  - Baseline Multi-Dataflow Composer
  - Static Power: Structural Optimization
  - Dynamic Power: Behavior Optimization
- Performance Assessment
  - Design Under Test
  - Structural Evaluation
  - Behavior Evaluation
- Final Remarks and Future Directions

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PROBLEM STATEMENT

CONSUMER NEEDS:

- **HIGH PERFORMANCES** real time applications:
  - Media players, video calling…
- **UP-TO-DATE SOLUTIONS**
  - Support for the last audio/video codecs, file formats…
- **MORE INTEGRATED FEATURES** in mobile devices:
  - MP3, Camera, Video, GPS…
- **LONG BATTERY LIFE**
  - Convenient form factor, affordable price…

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POSSIBLE SOLUTION:

- **DATAFLOW MODEL OF COMPUTATION**
  - Modularity and parallelism → **EASIER INTEGRATION AND FAVOURED RE-USABILITY**
- **COARSE-GRAINED RECONFIGURABILITY**
  - Flexibility and resource sharing → **MULTI-APPLICATION PORTABLE DEVICES**

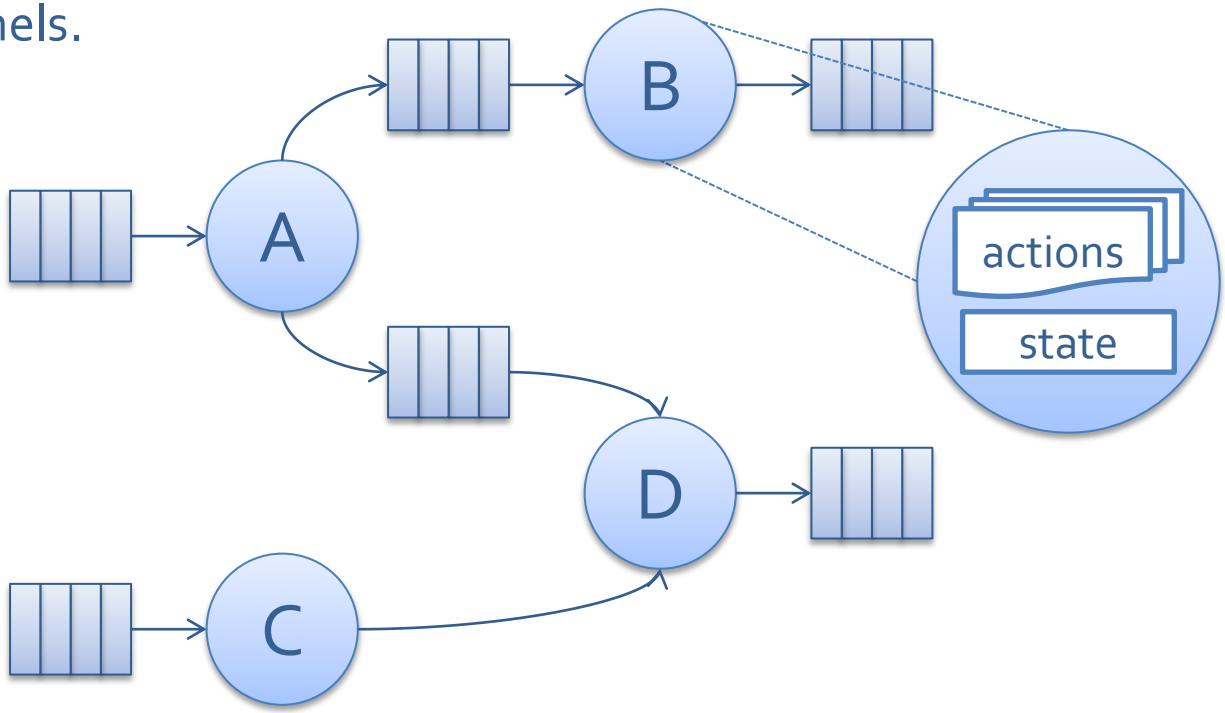
BACKGROUND

DATAFLOW FORMALISM

- Directed graph of **actors** (functional units).
- Actors exchange **tokens** (data packets) through dedicated channels.

CHARATERISTICS

- Explicit the intrinsic application **parallelism**.
- Modularity favours model **long-term adaptivity**.



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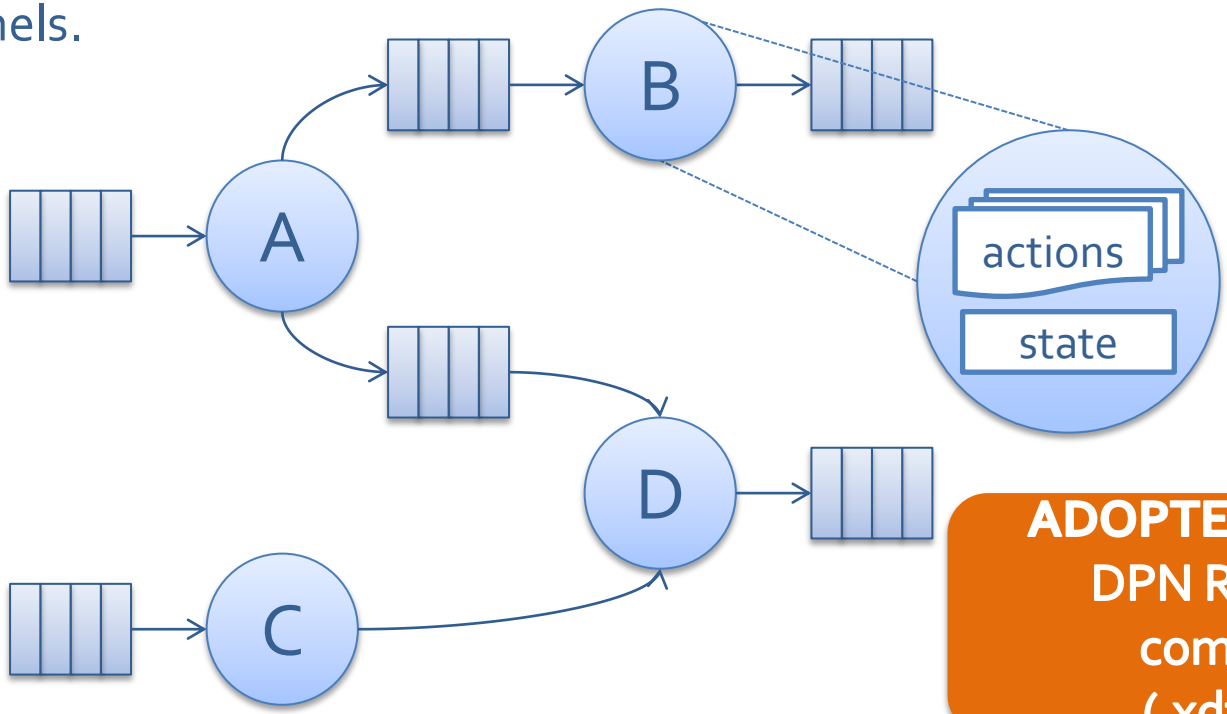


ADOPTED MODEL:
DPN RVC-CAL compliant (.xdf, .cal)

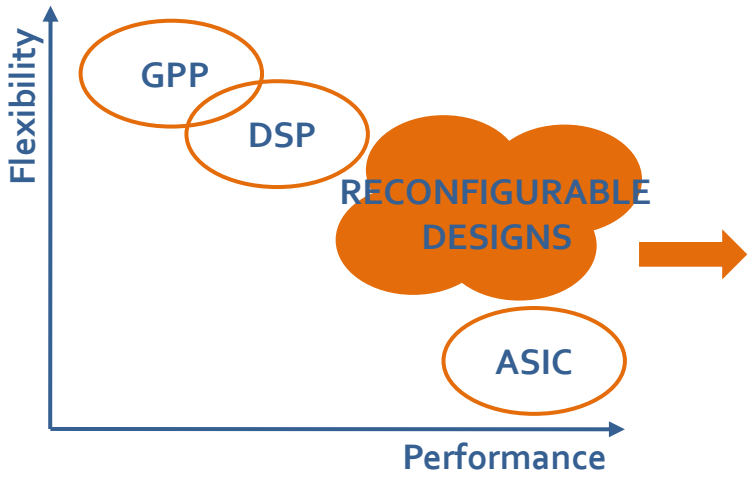
BACKGROUND

FINE- GRAINED (FG) RECONFIGURATION

- High flexibility bit-level reconfiguration
- Slow and memory expensive configuration phase
- Suitable for applications with high control flow

COARSE-GRAINED (CG) RECONFIGURATION

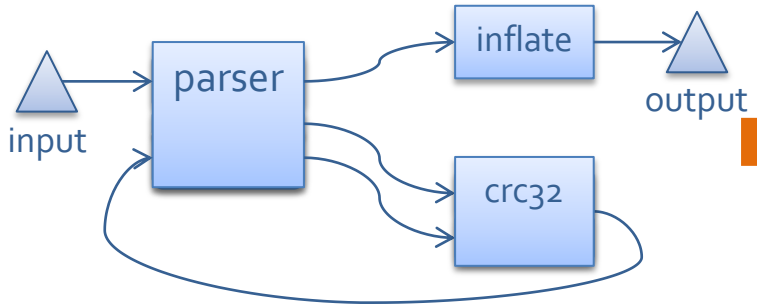
- Medium flexibility word-level reconfiguration
- Fast configuration phase
- Suitable for applications with high level of instruction/data parallelism



	FG	CG
	Bit-level	Word-level
Flexibility	☺	😐
Reconf. Speed	😐	☺
Config. Storage	☹	😐

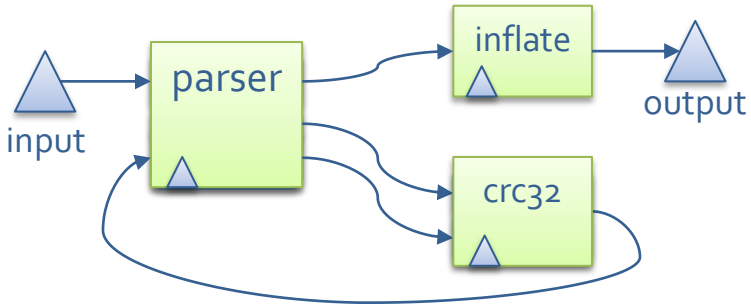
BACKGROUND

RVC-Cal Dataflow Description (DPN)

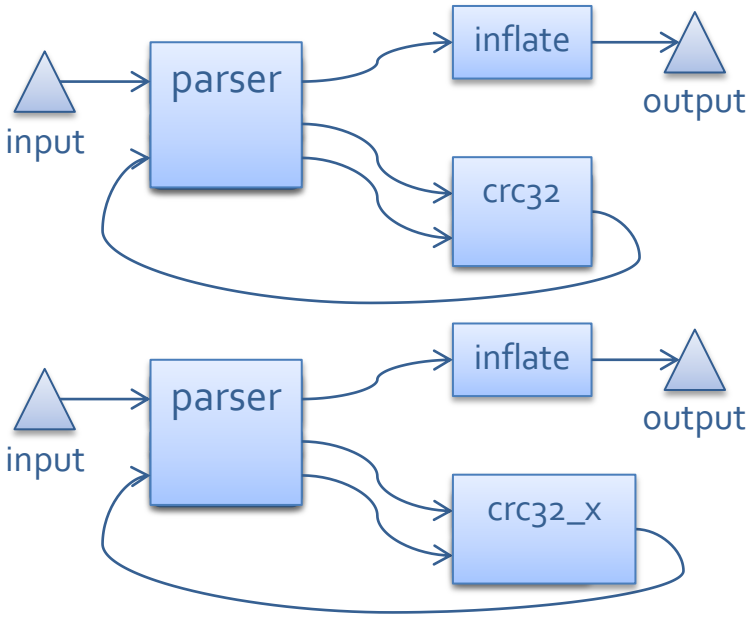


1:1

Coarse Grained HardwarePlatform

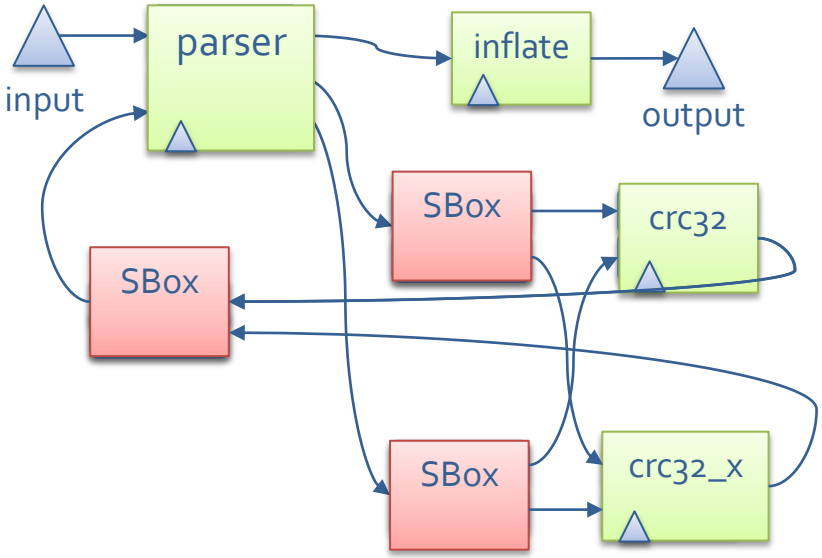


RVC-Cal Dataflow Descriptions (DPNs)

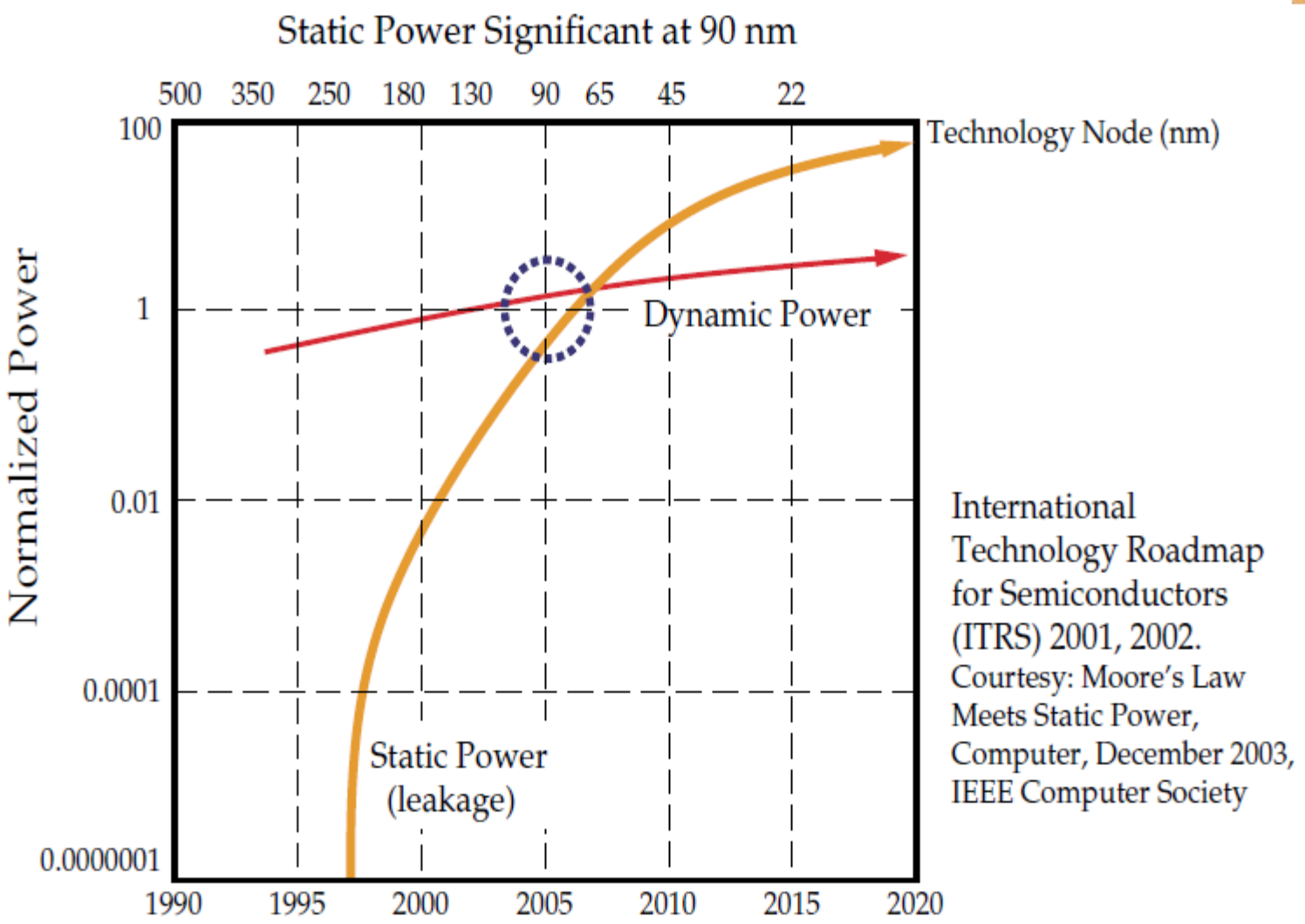


2:1

Coarse Grained Reconfigurable HardwarePlatform



THE POWER ISSUE



International Technology Roadmap for Semiconductors (ITRS) 2001, 2002.
Courtesy: Moore's Law Meets Static Power, Computer, December 2003, IEEE Computer Society

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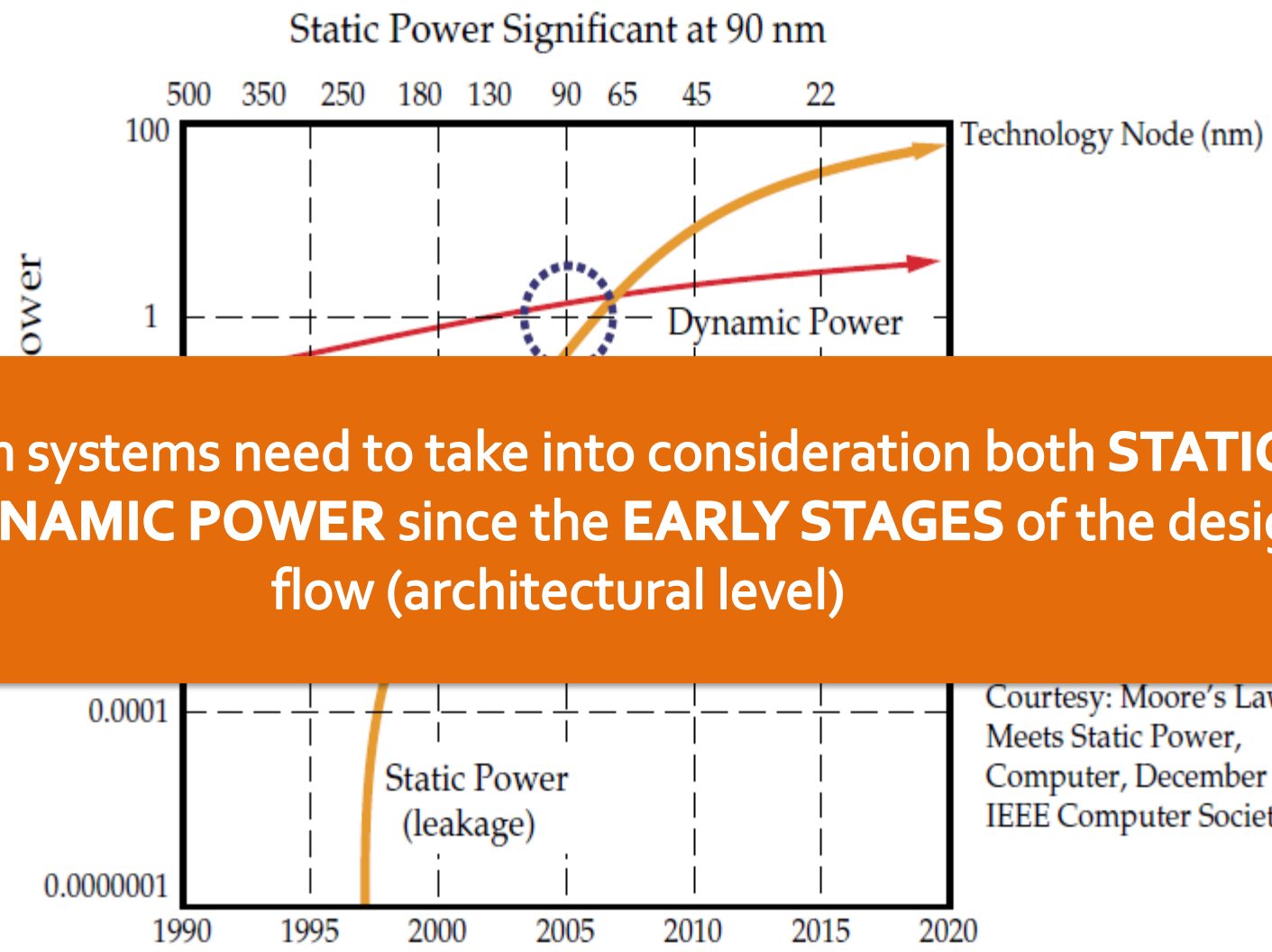

Modern systems need to take into consideration both STATIC AND DYNAMIC POWER since the EARLY STAGES of the design flow (architectural level)

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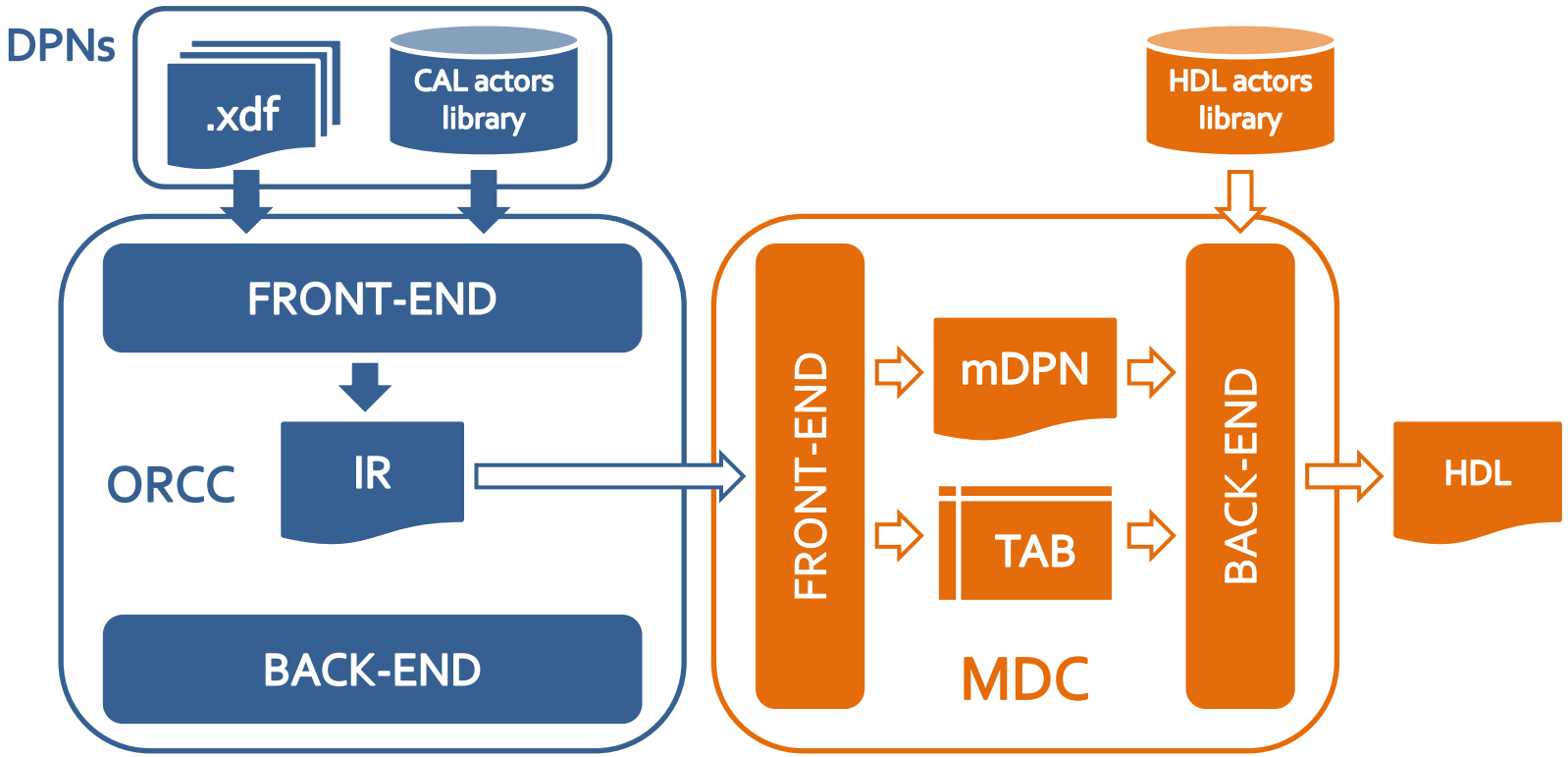
BASELINE MULTI-DATAFLOW COMPOSER



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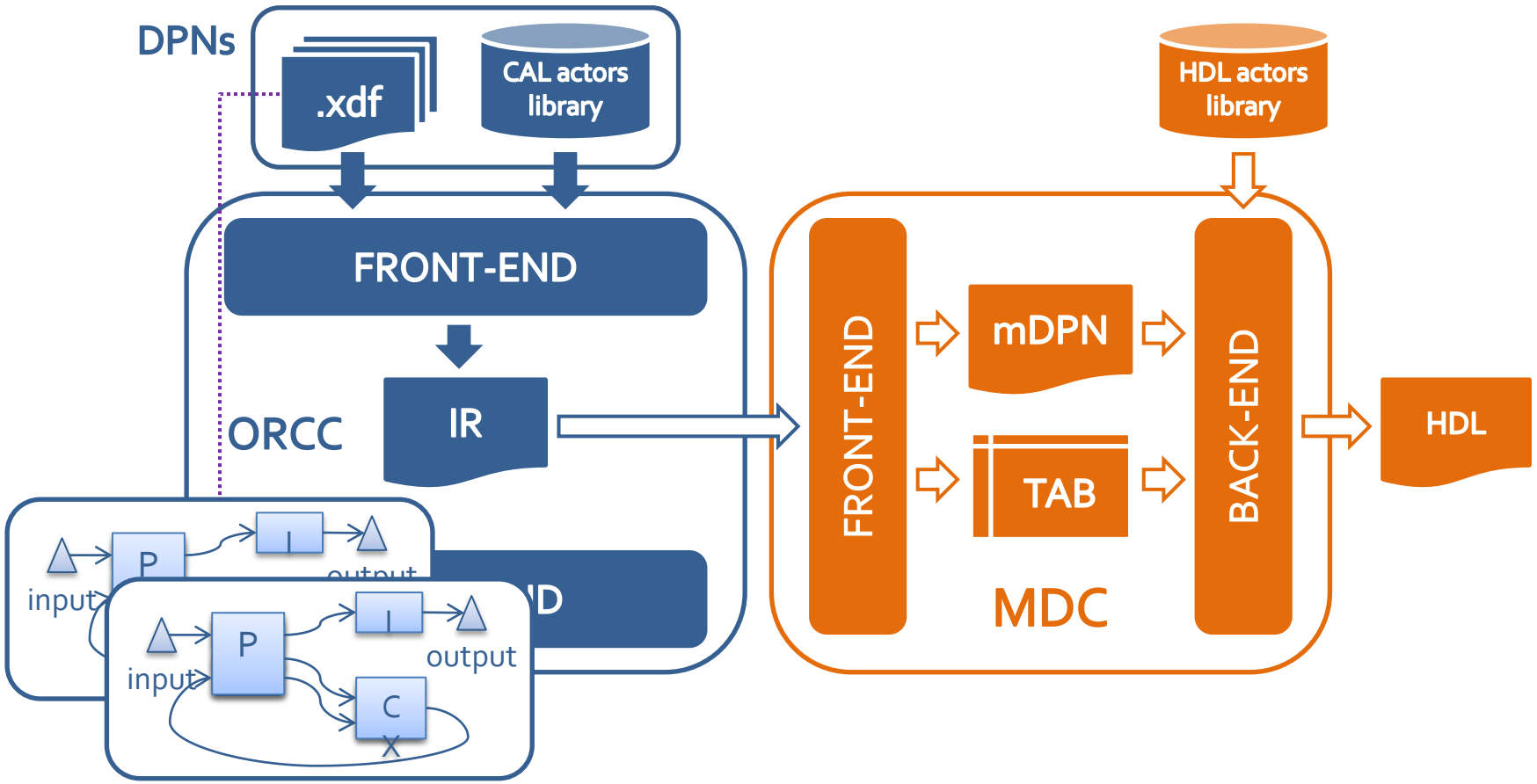

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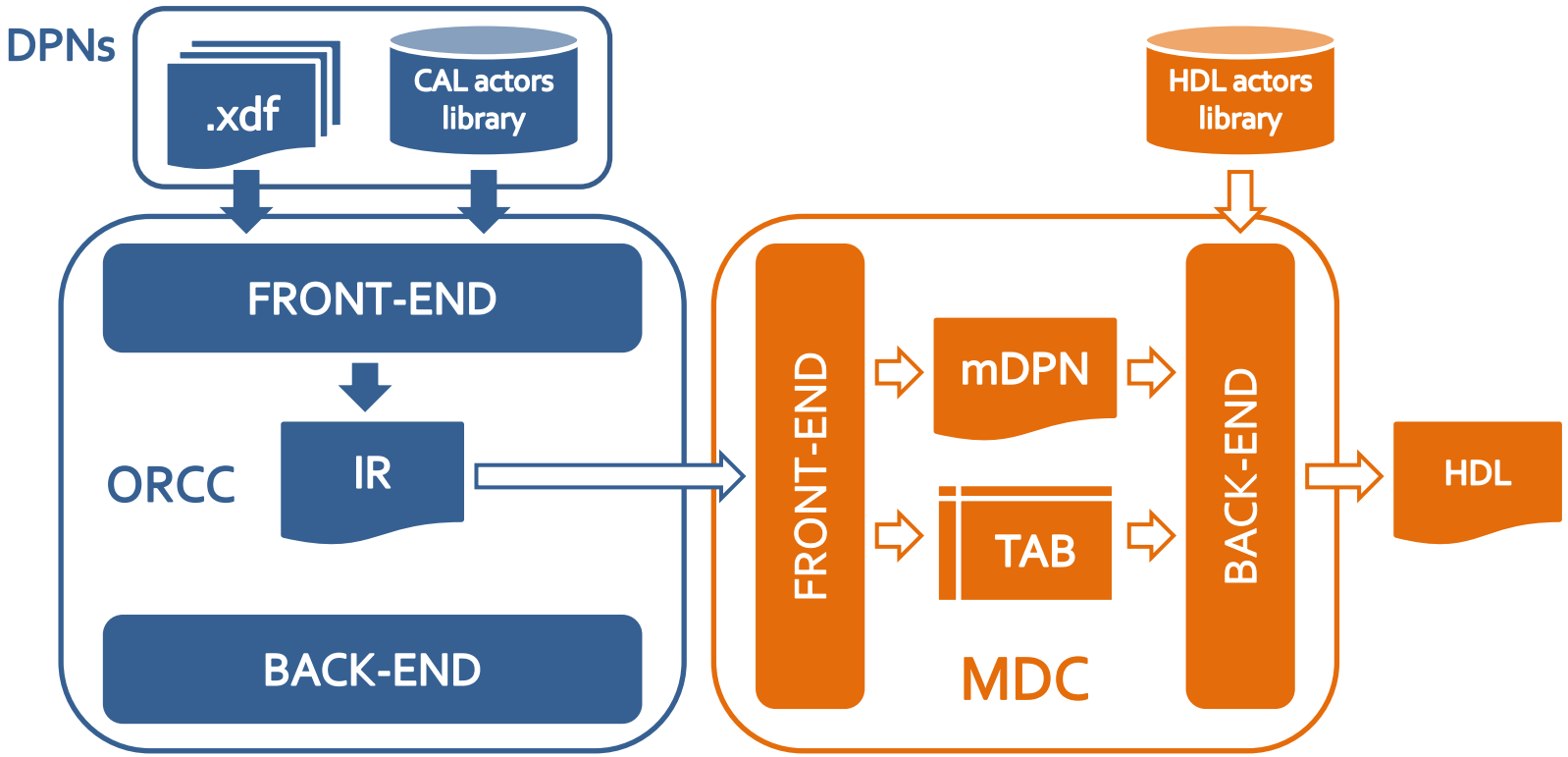

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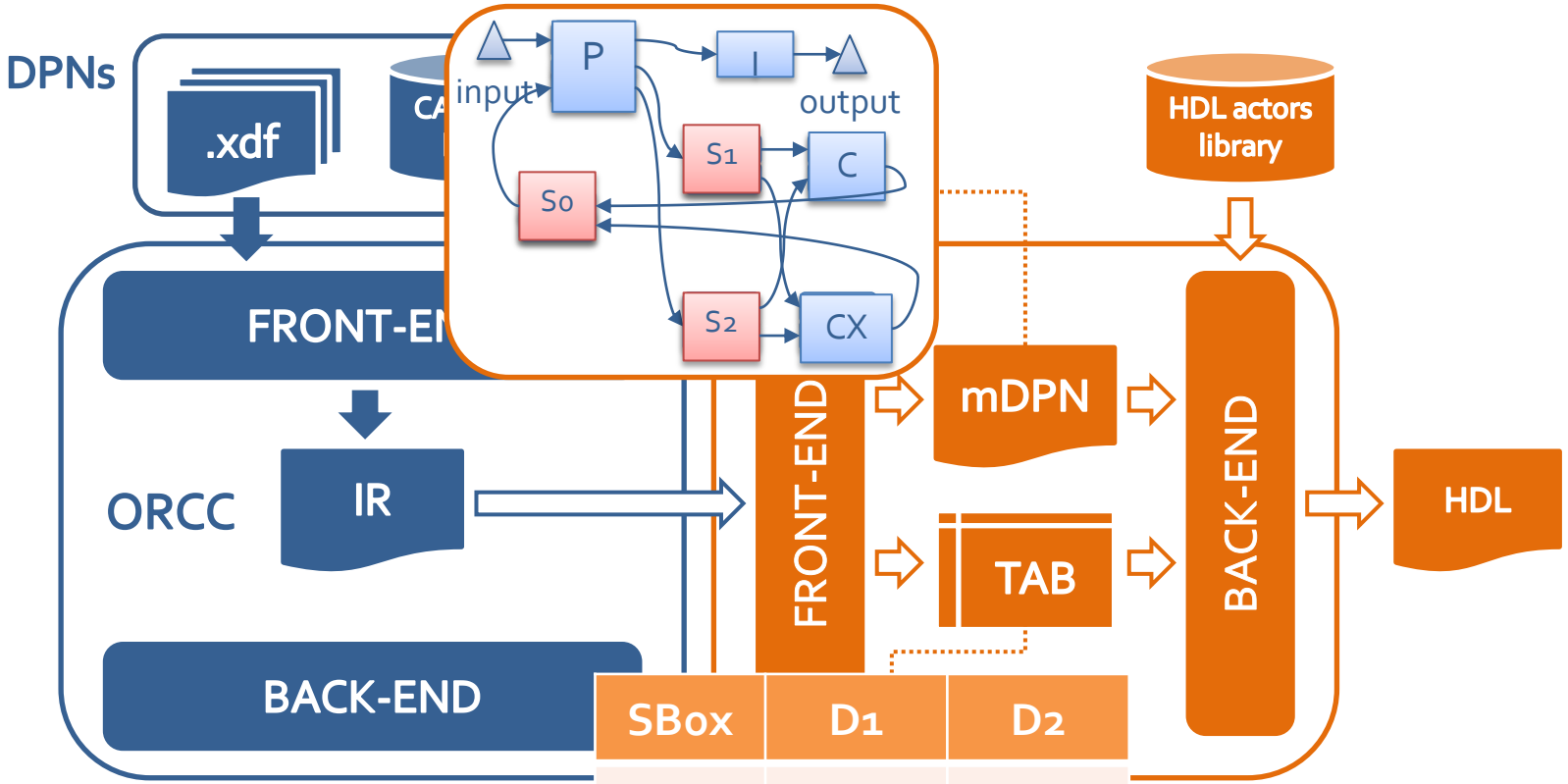

SBox	D1	D2
S0	0	1
S1	0	1
S2	0	1

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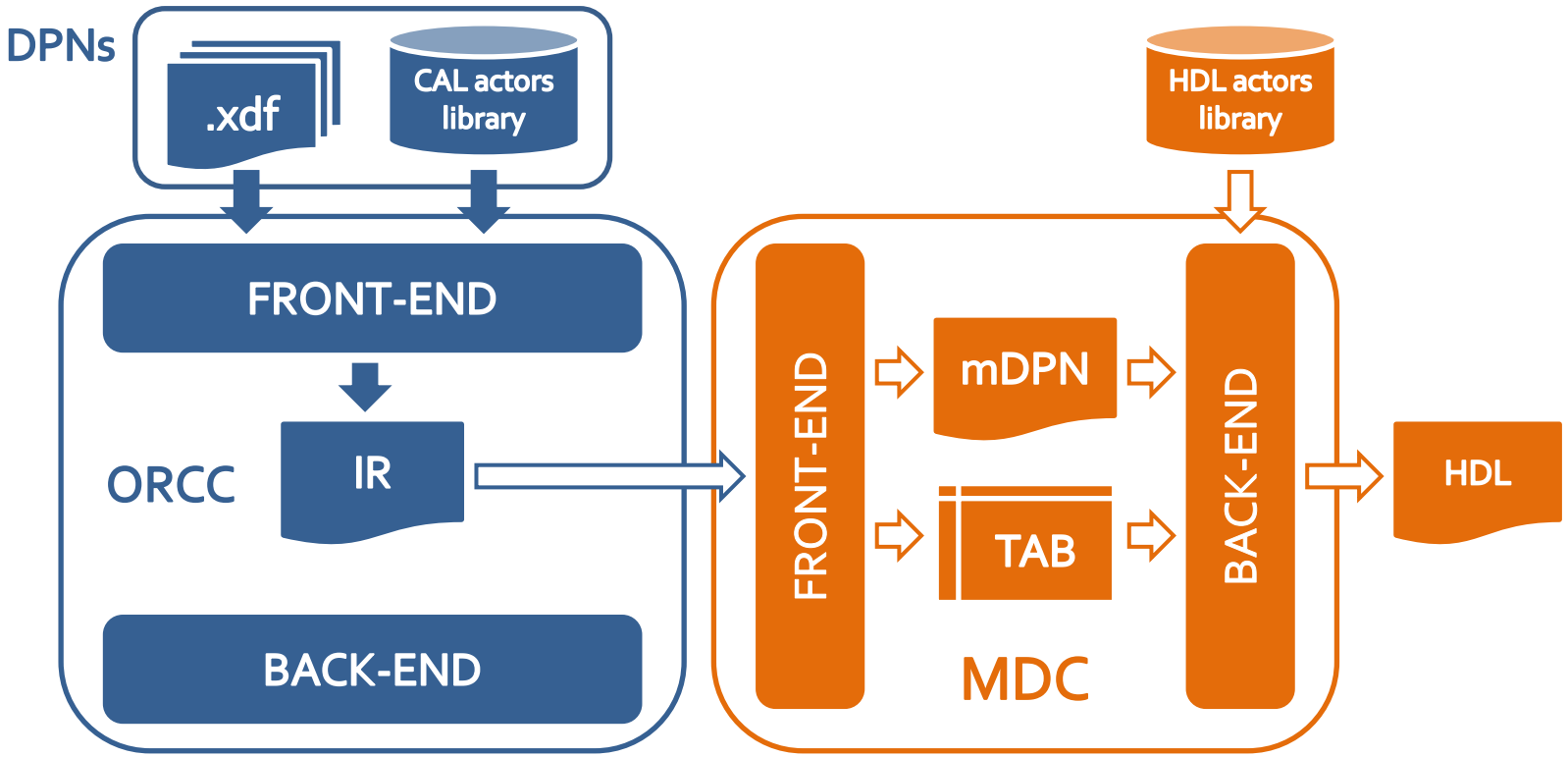

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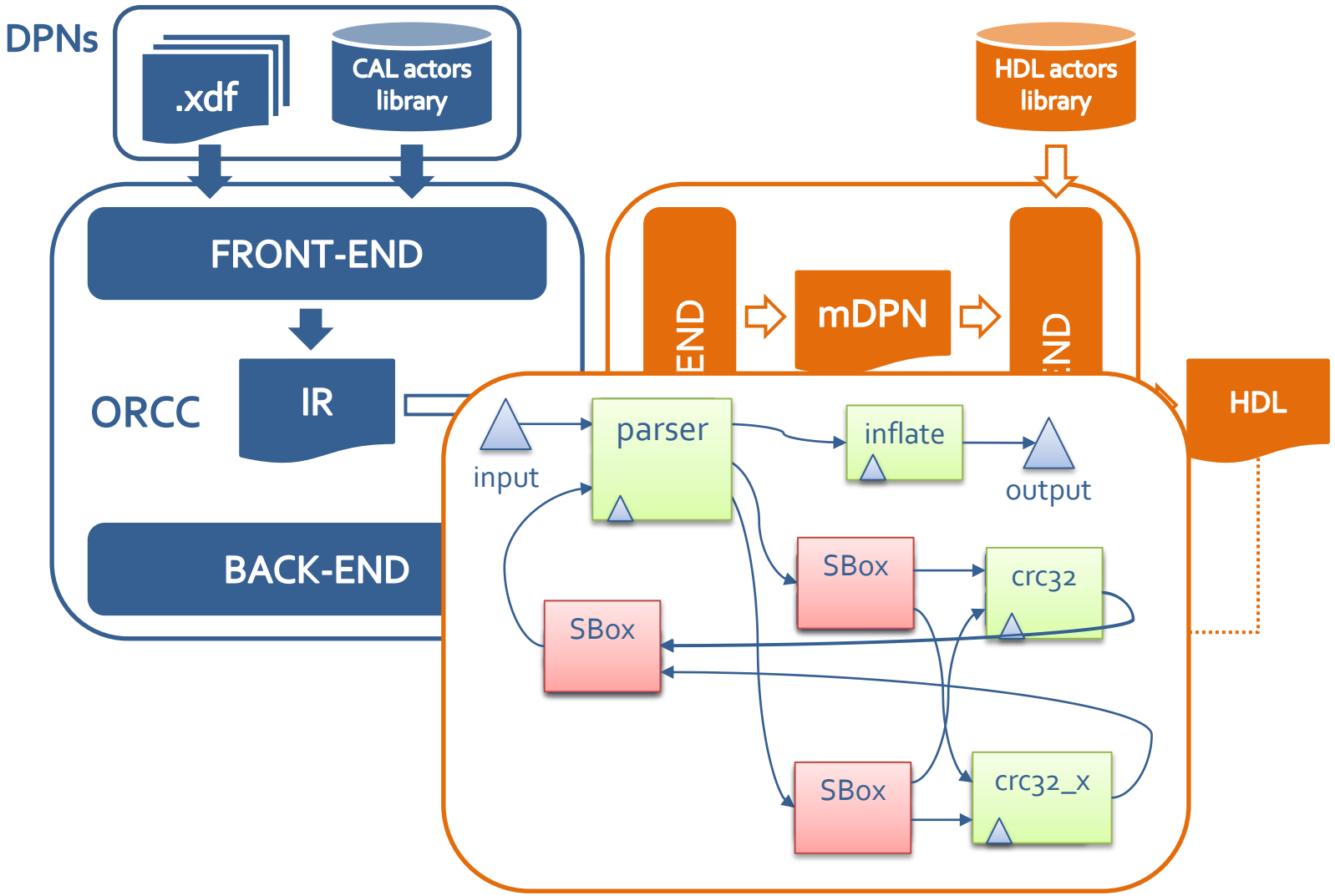
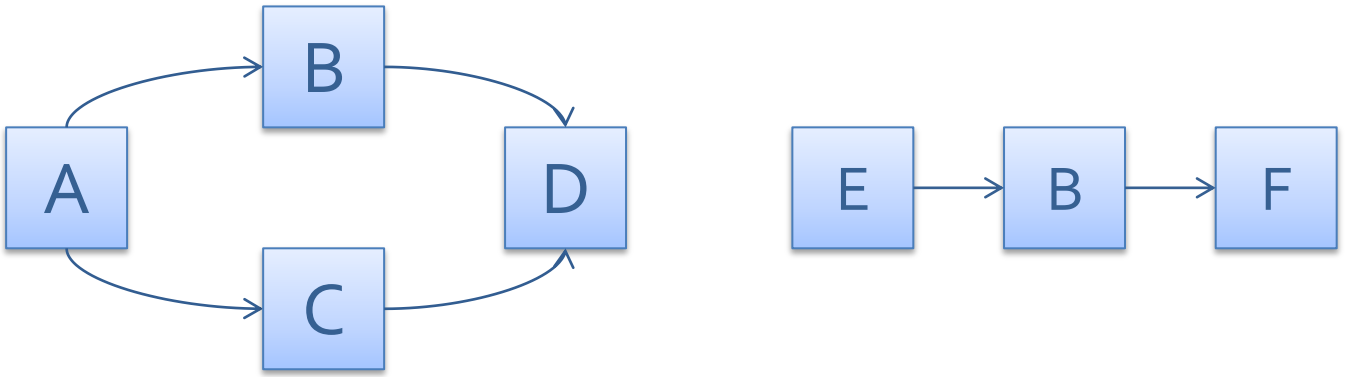


STATIC POWER MANAGEMENT: STRUCTURAL OPTIMIZATION



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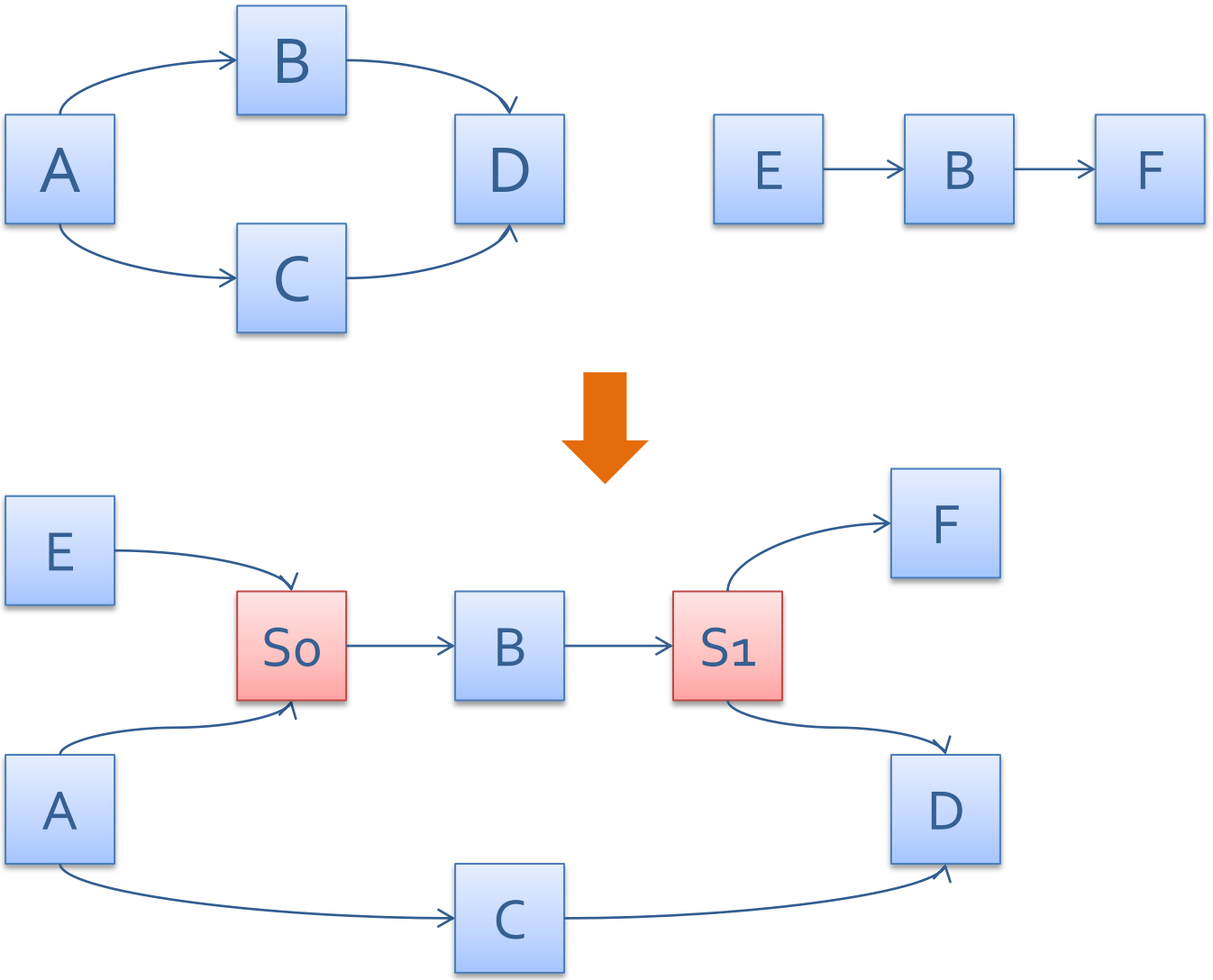

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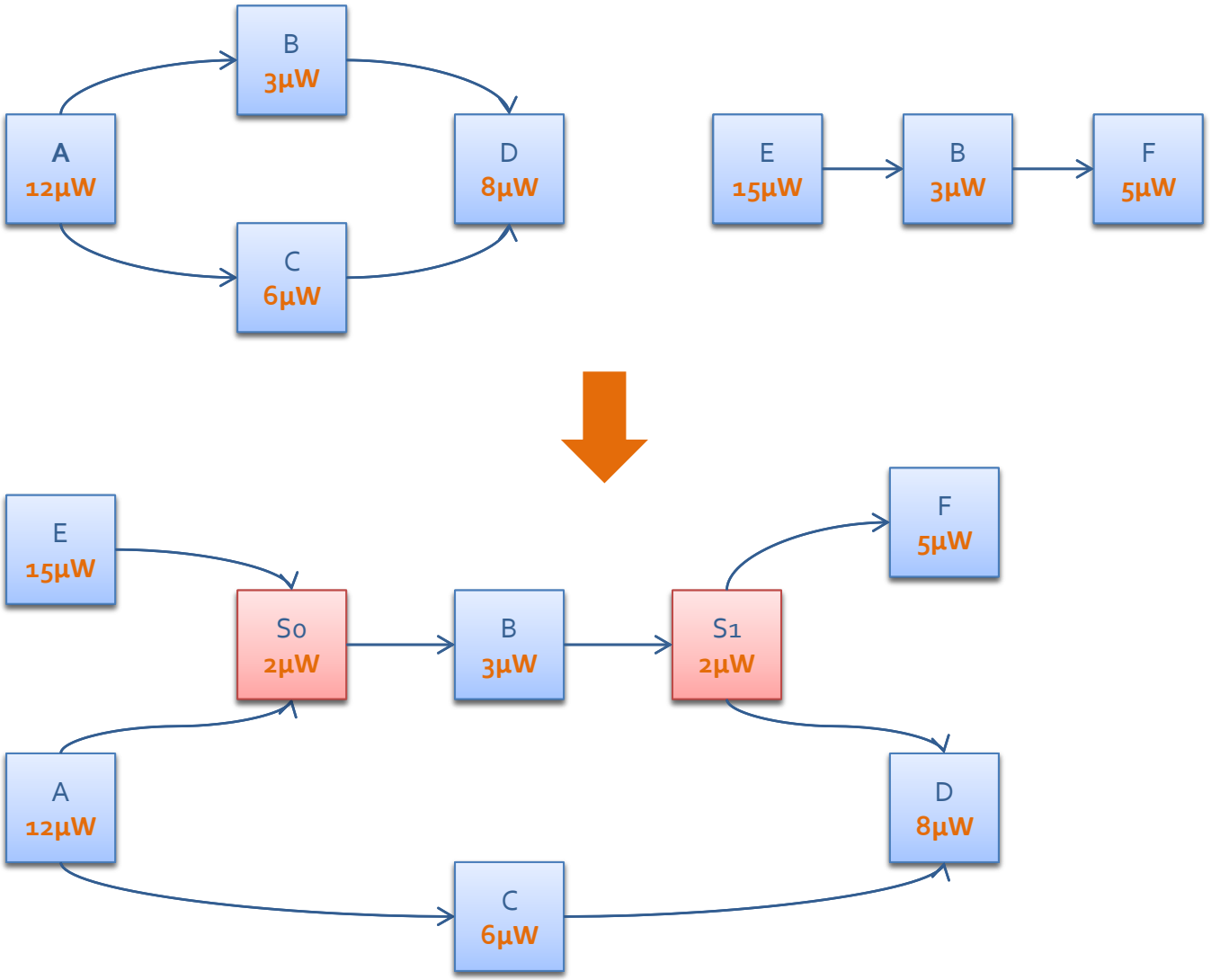

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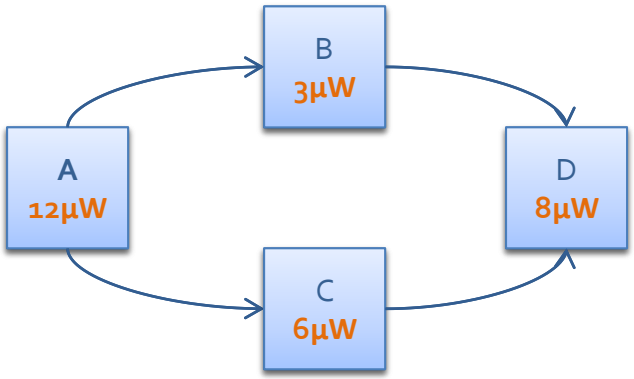
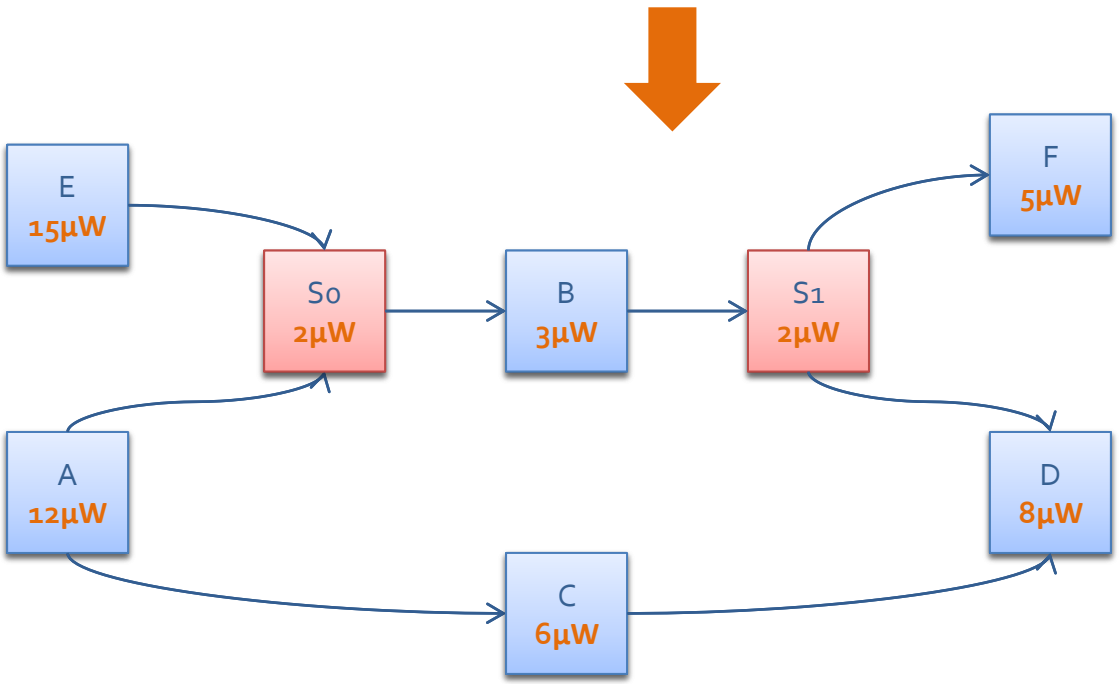


= 52µW



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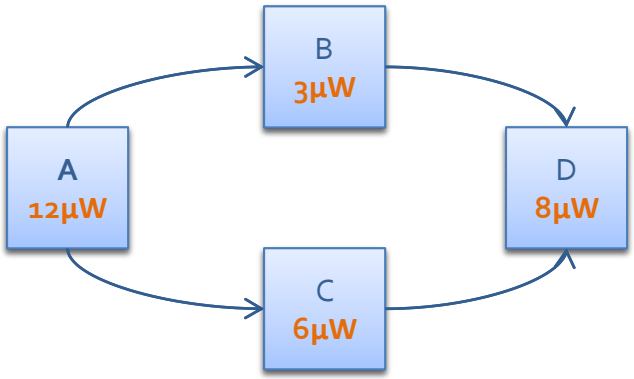

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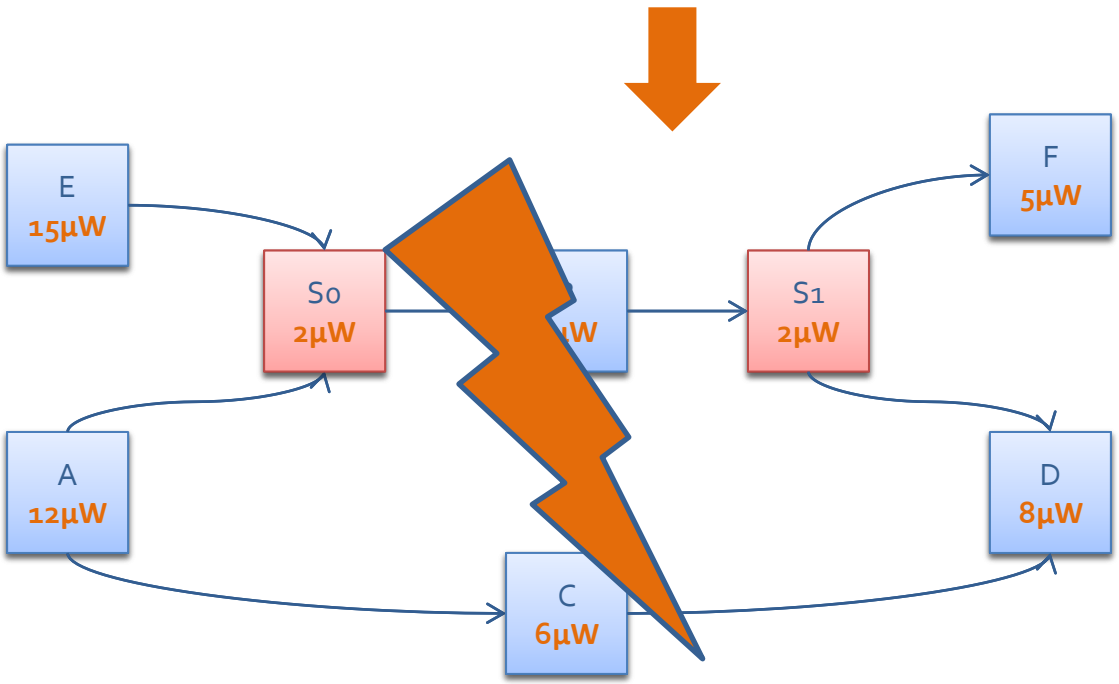

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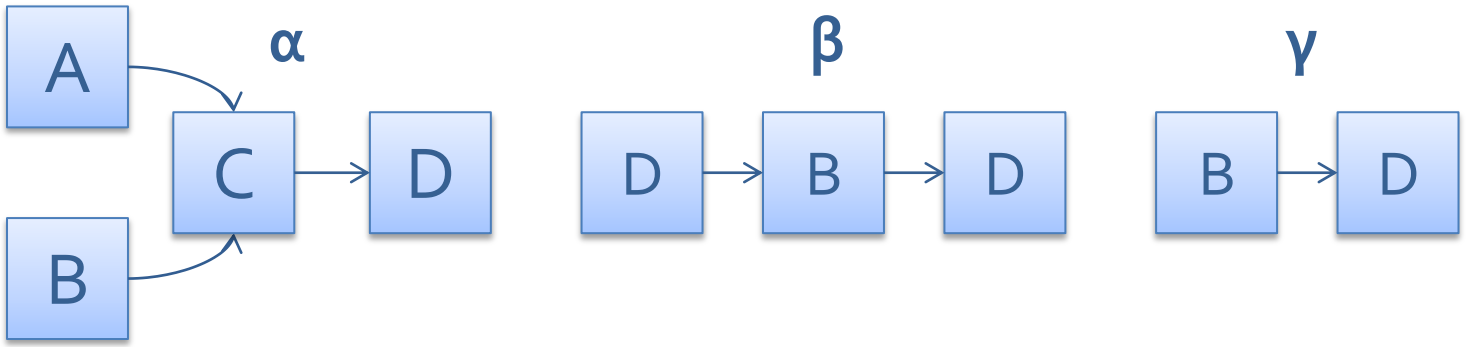

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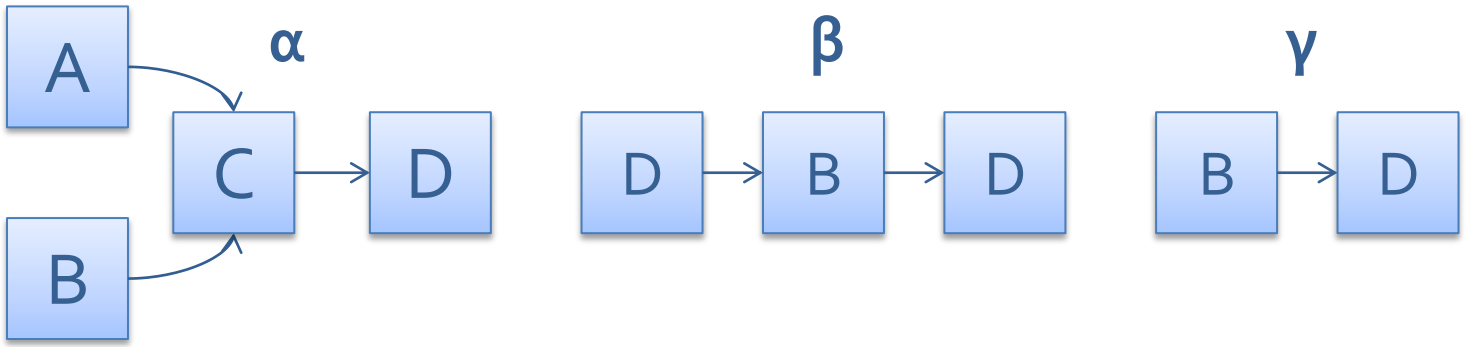

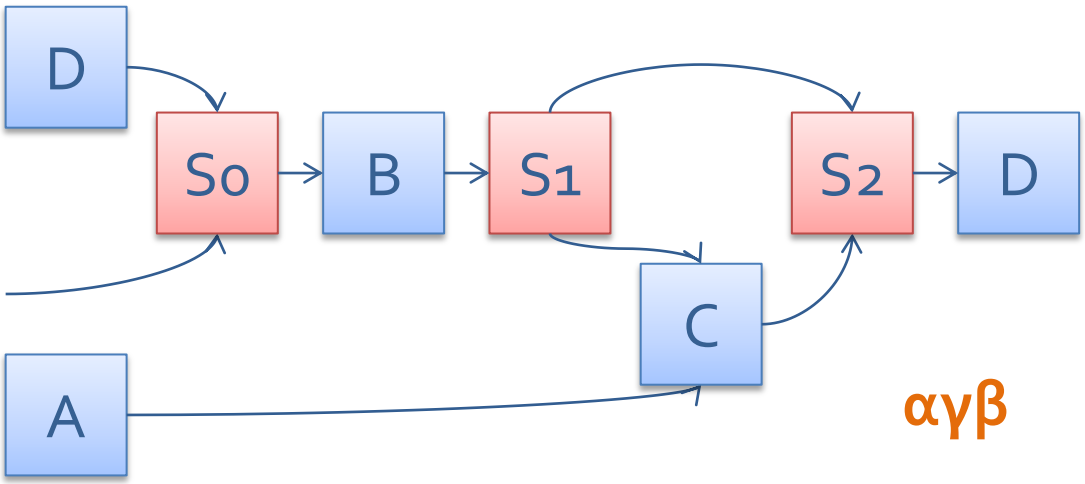

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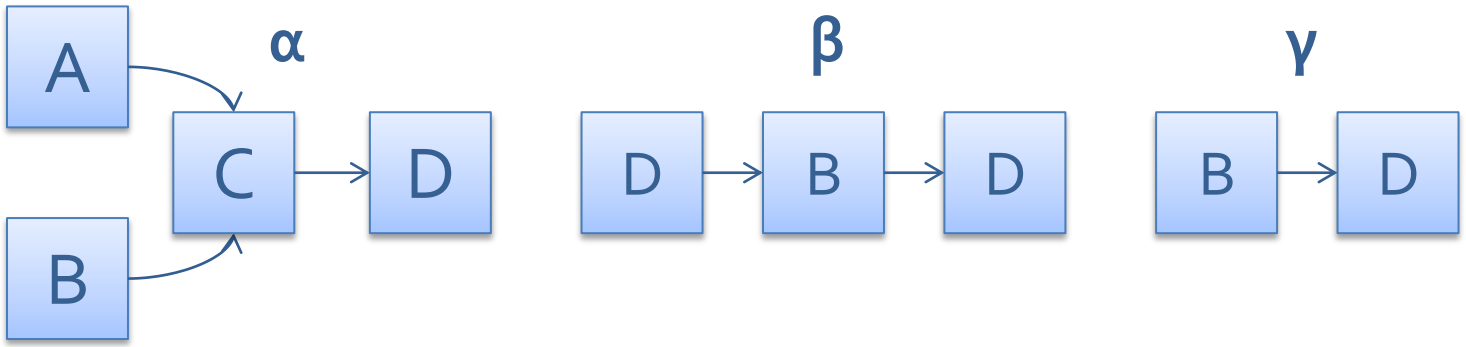

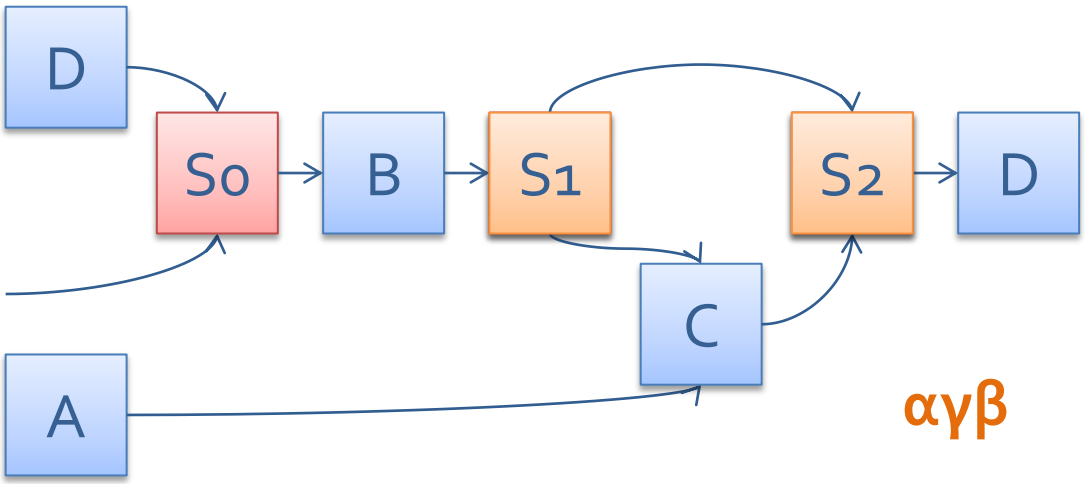

αγβ

longest chain 2 SBoxes

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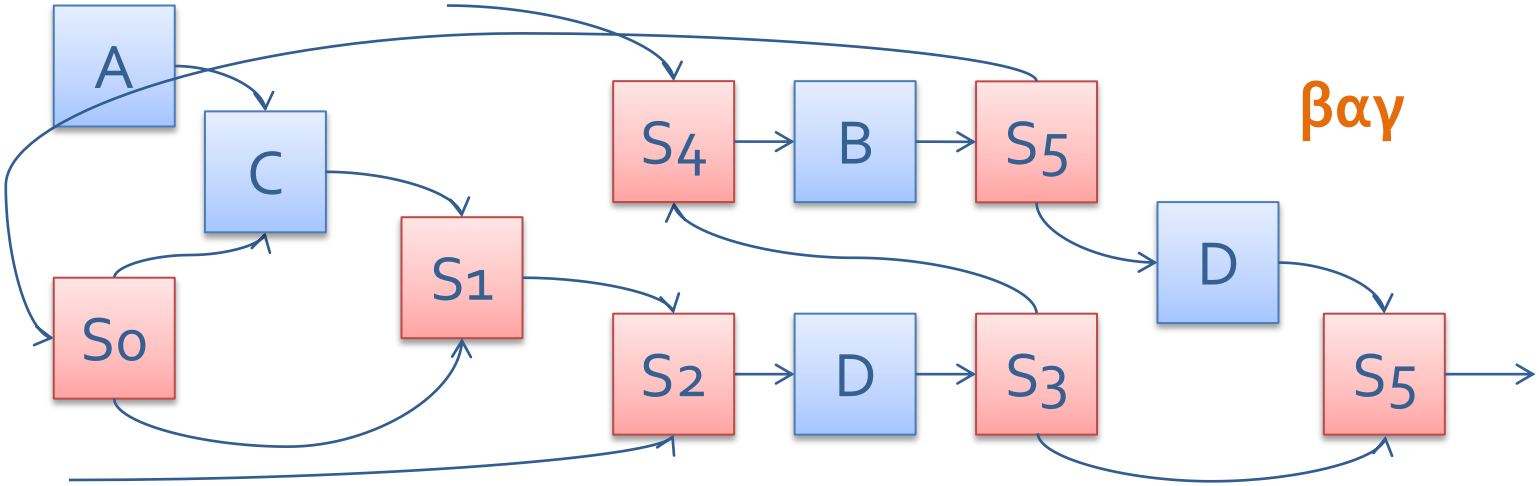
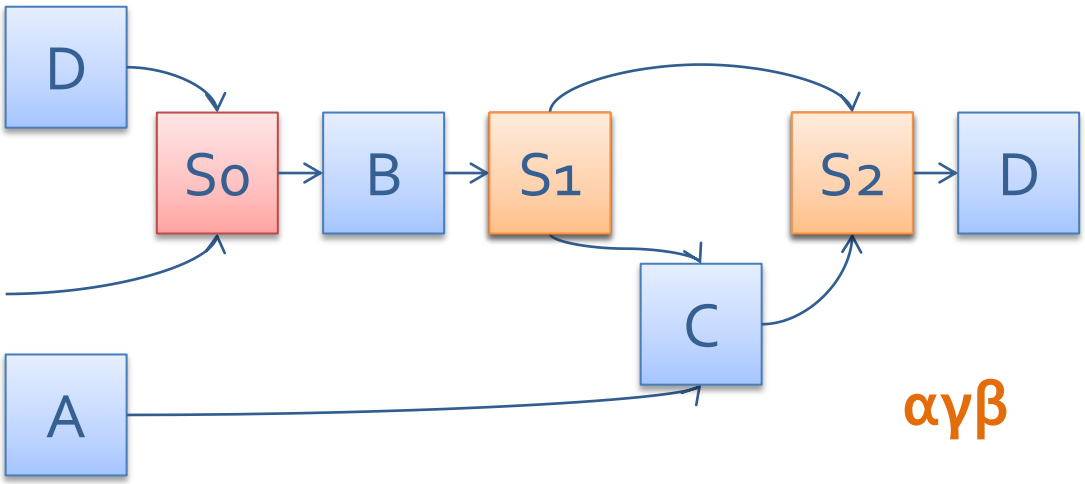


βαγ



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longest chain
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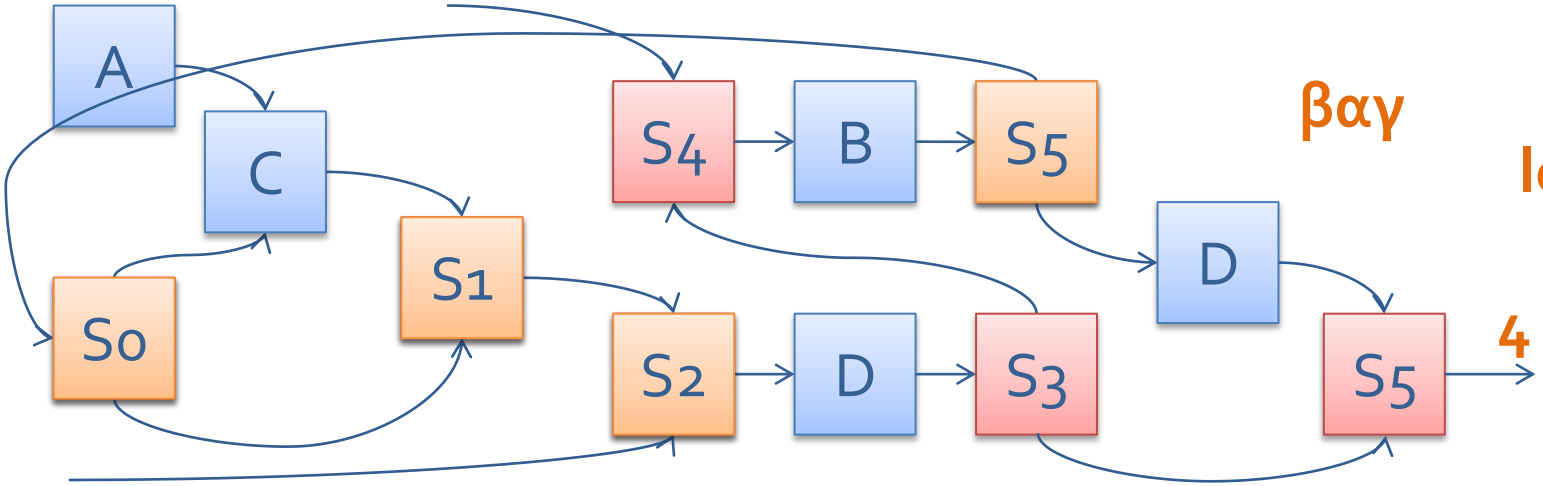
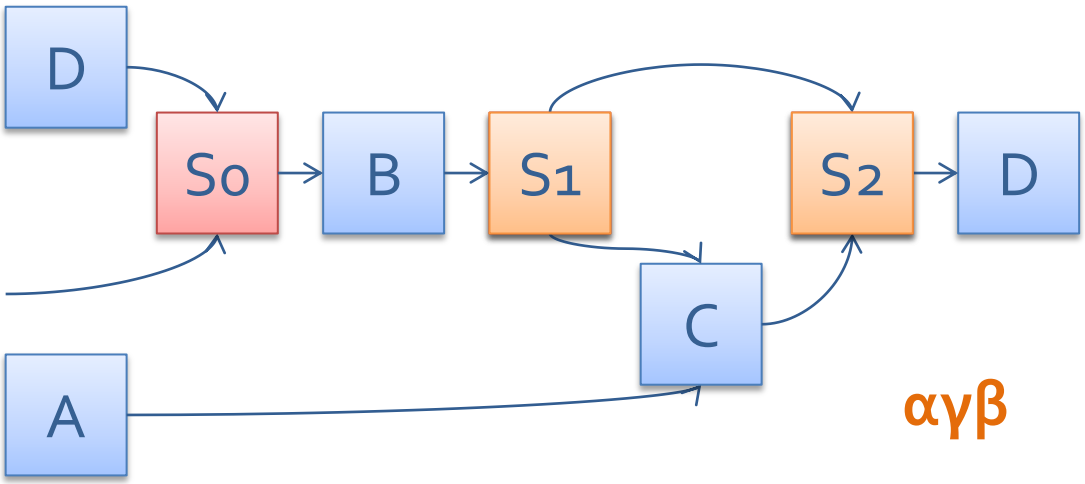


βαγ

longest chain 4 SBoxes



αγβ

longest chain 2 SBoxes

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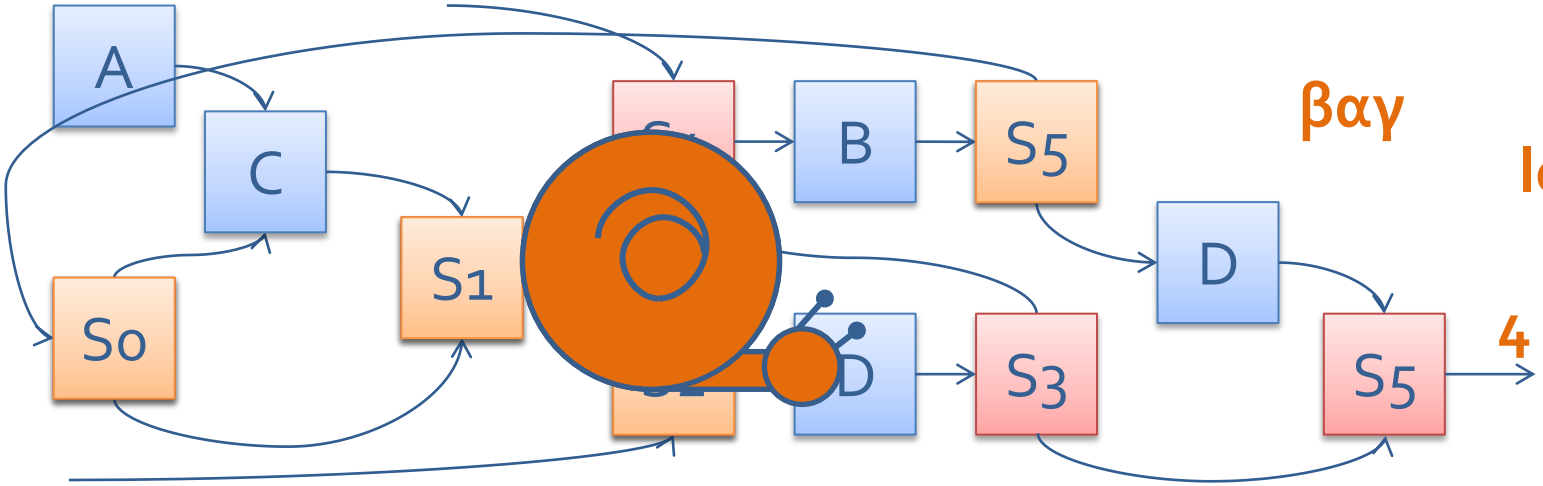

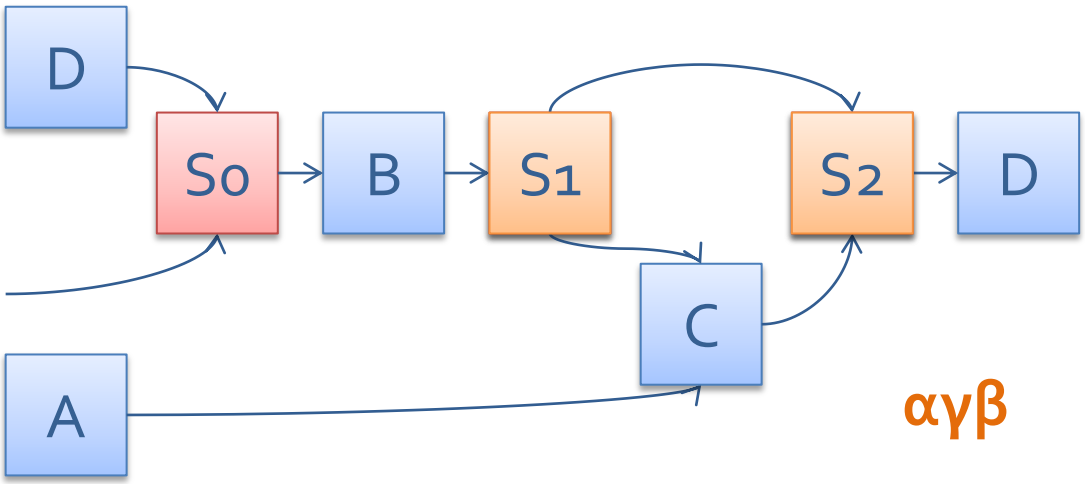

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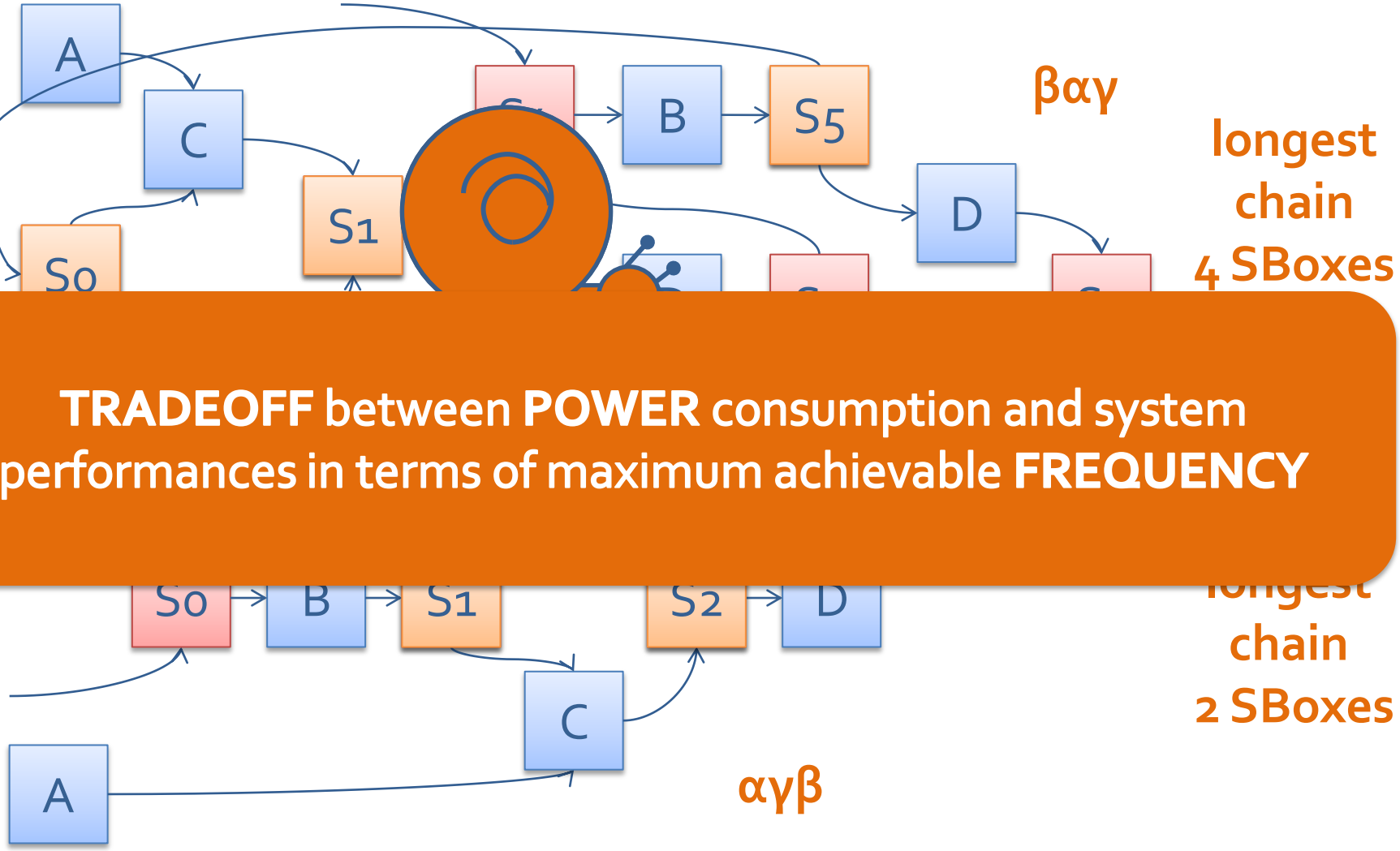

TRADEOFF between **POWER** consumption and system performances in terms of maximum achievable **FREQUENCY**

STATIC POWER MANAGEMENT: STRUCTURAL OPTIMIZATION

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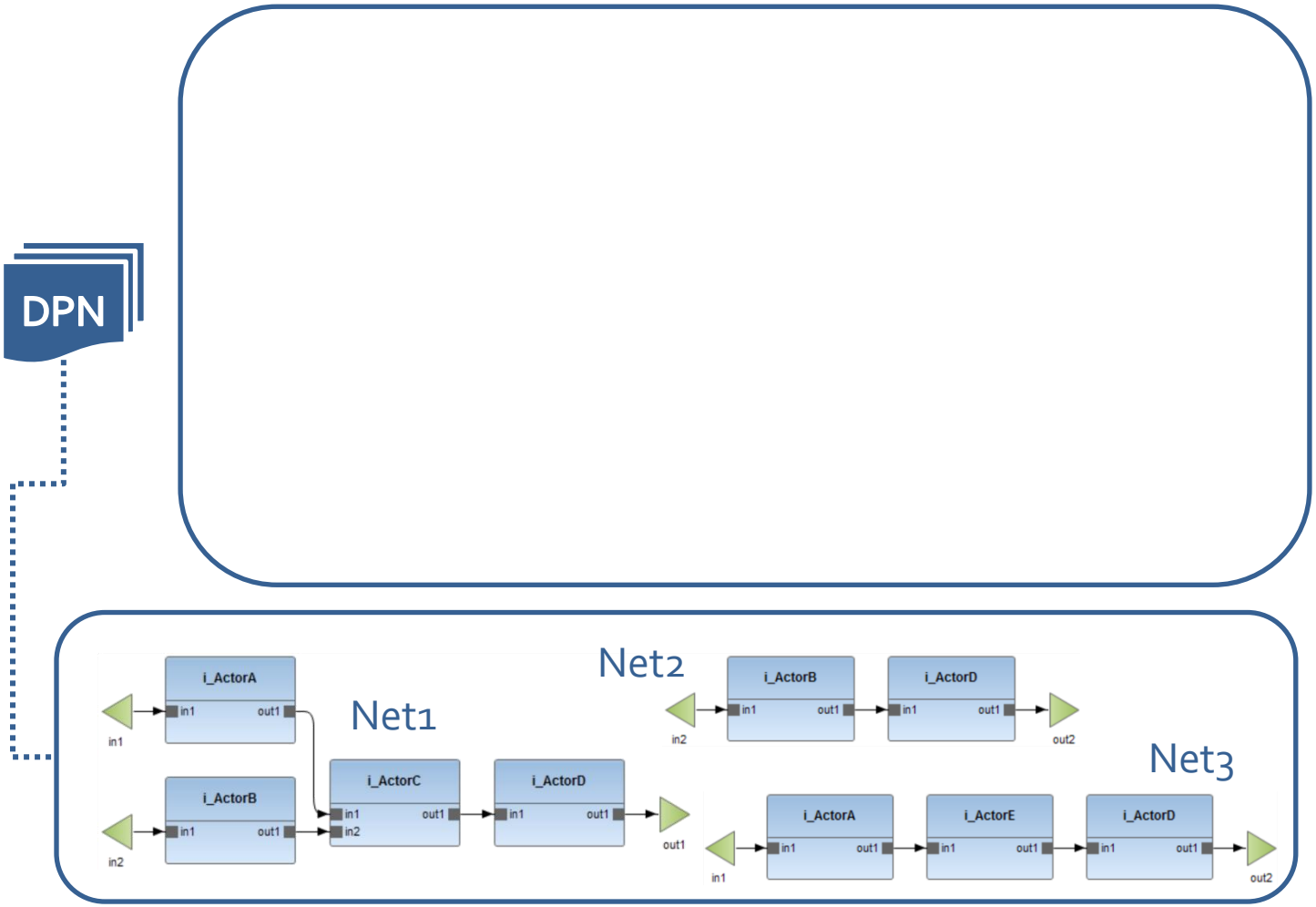

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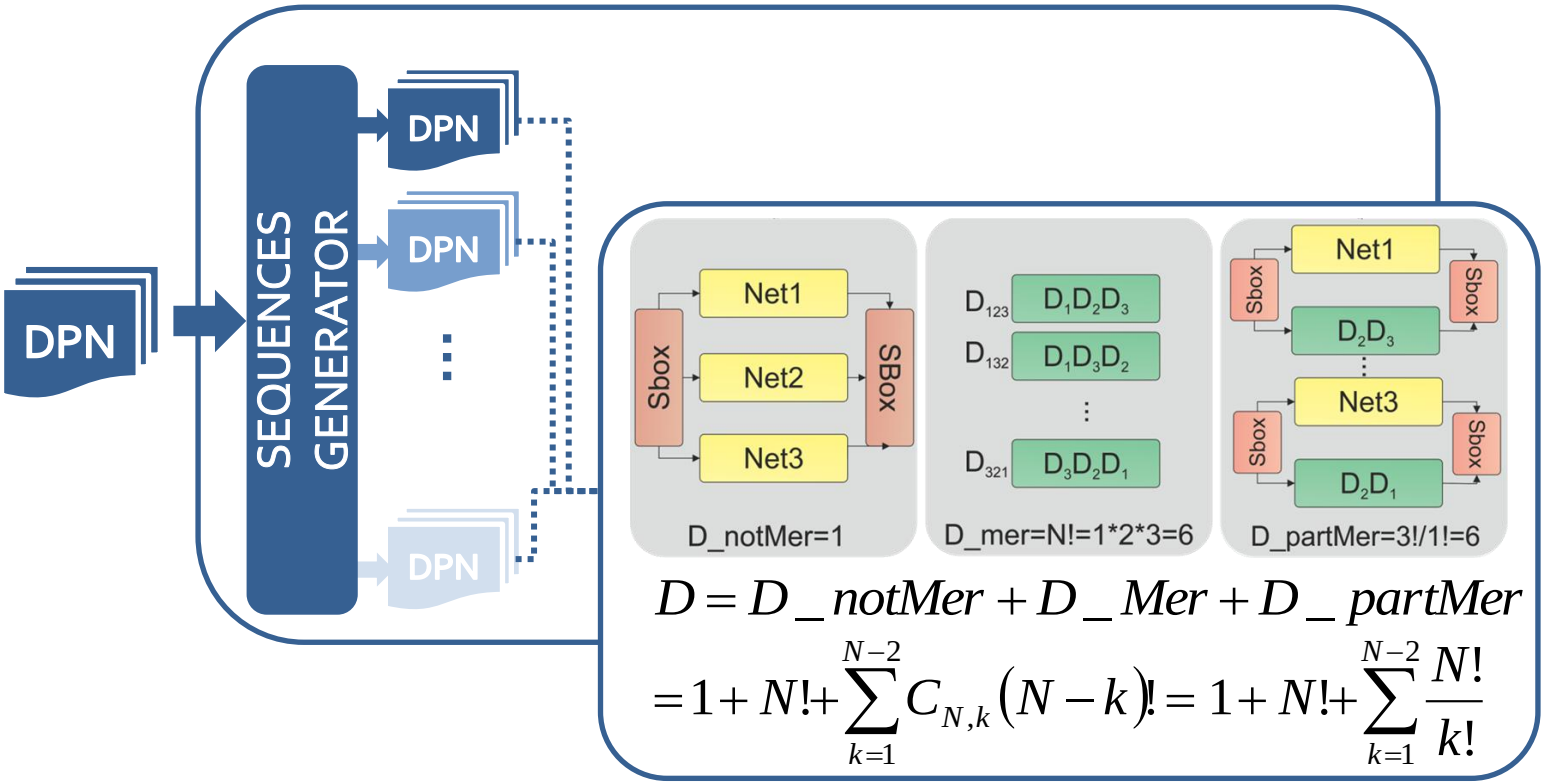

$$D = D\_notMer + D\_Mer + D\_partMer$$
$$= 1 + N! + \sum_{k=1}^{N-2} C_{N,k}(N-k)! = 1 + N! + \sum_{k=1}^{N-2} \frac{N!}{k!}$$

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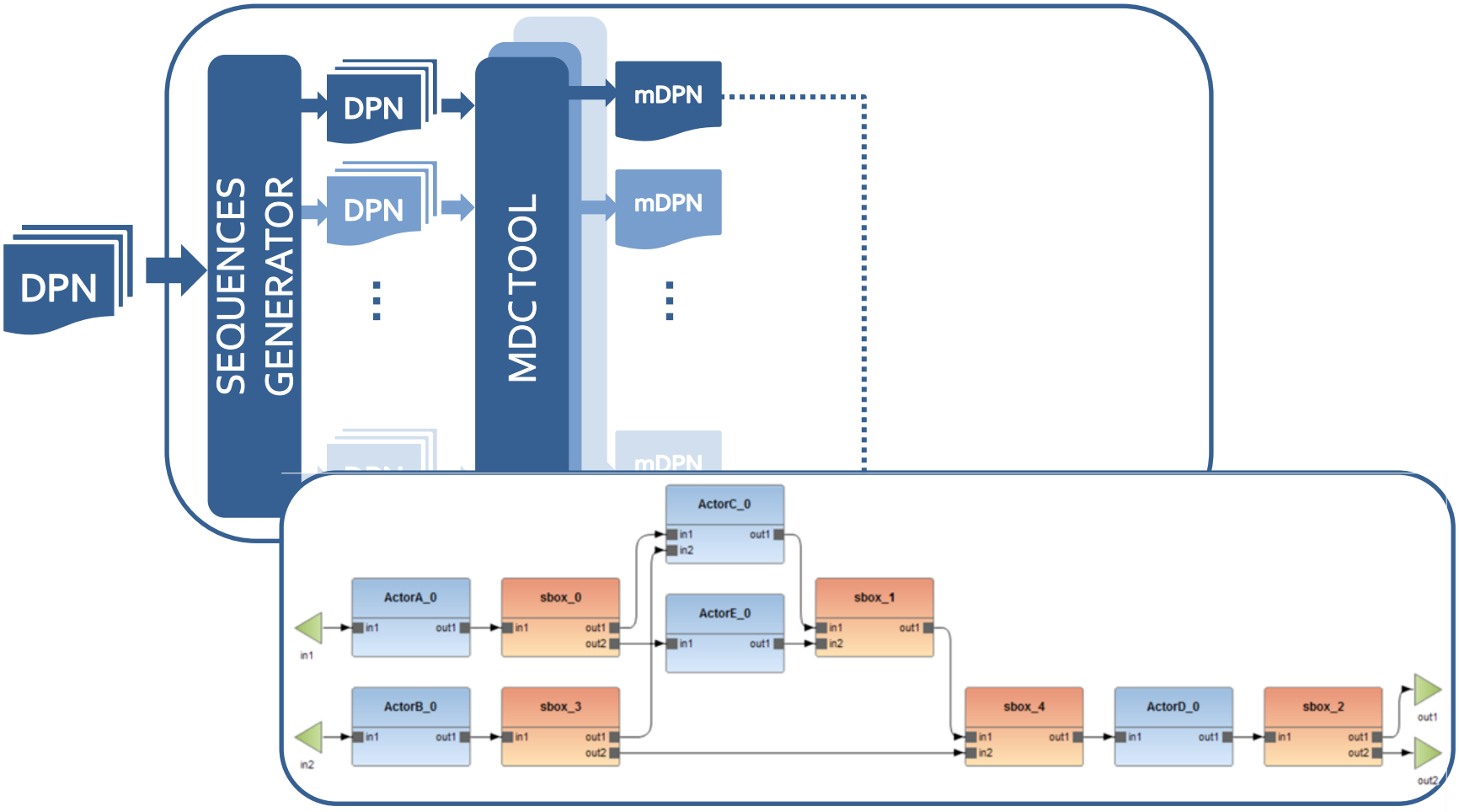

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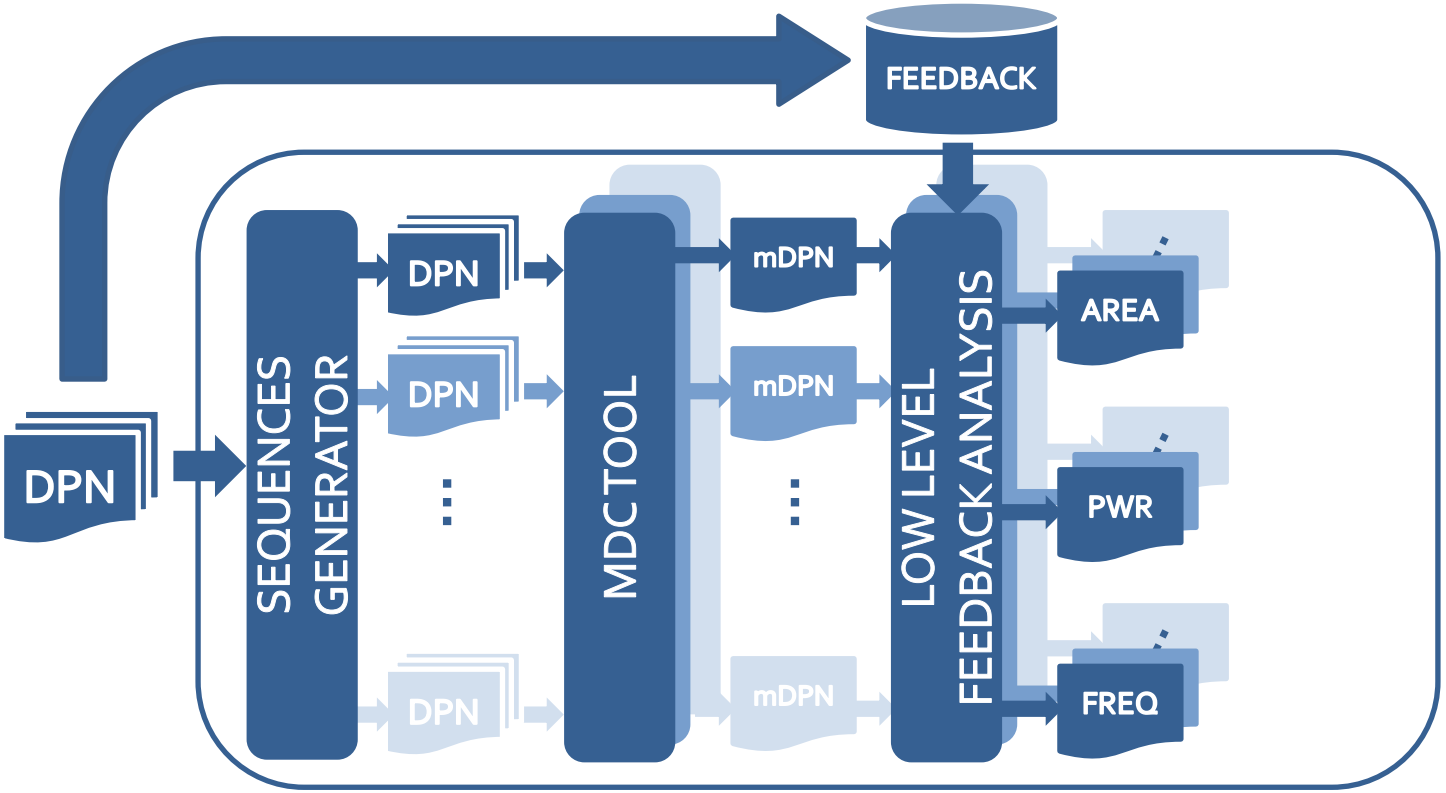

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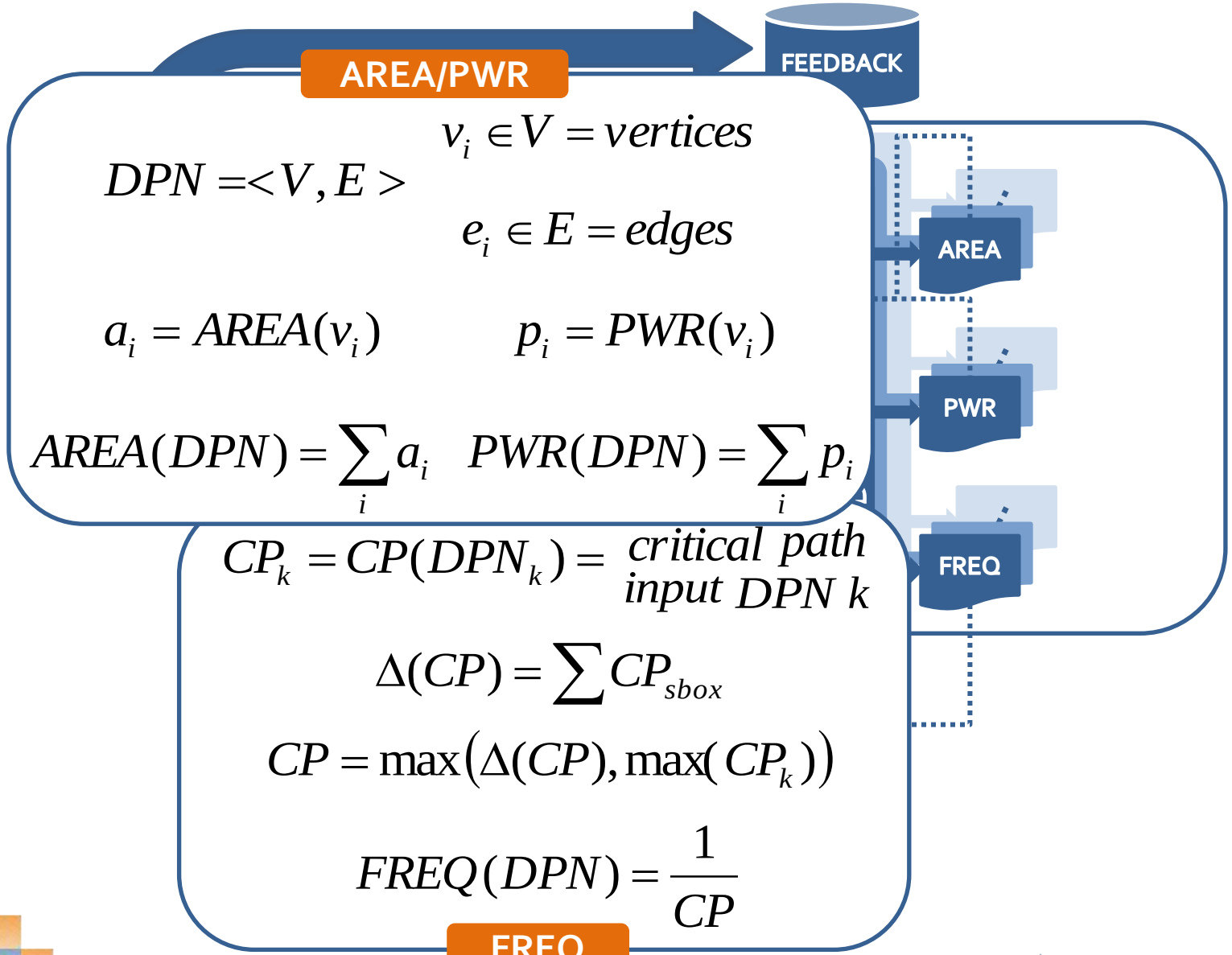

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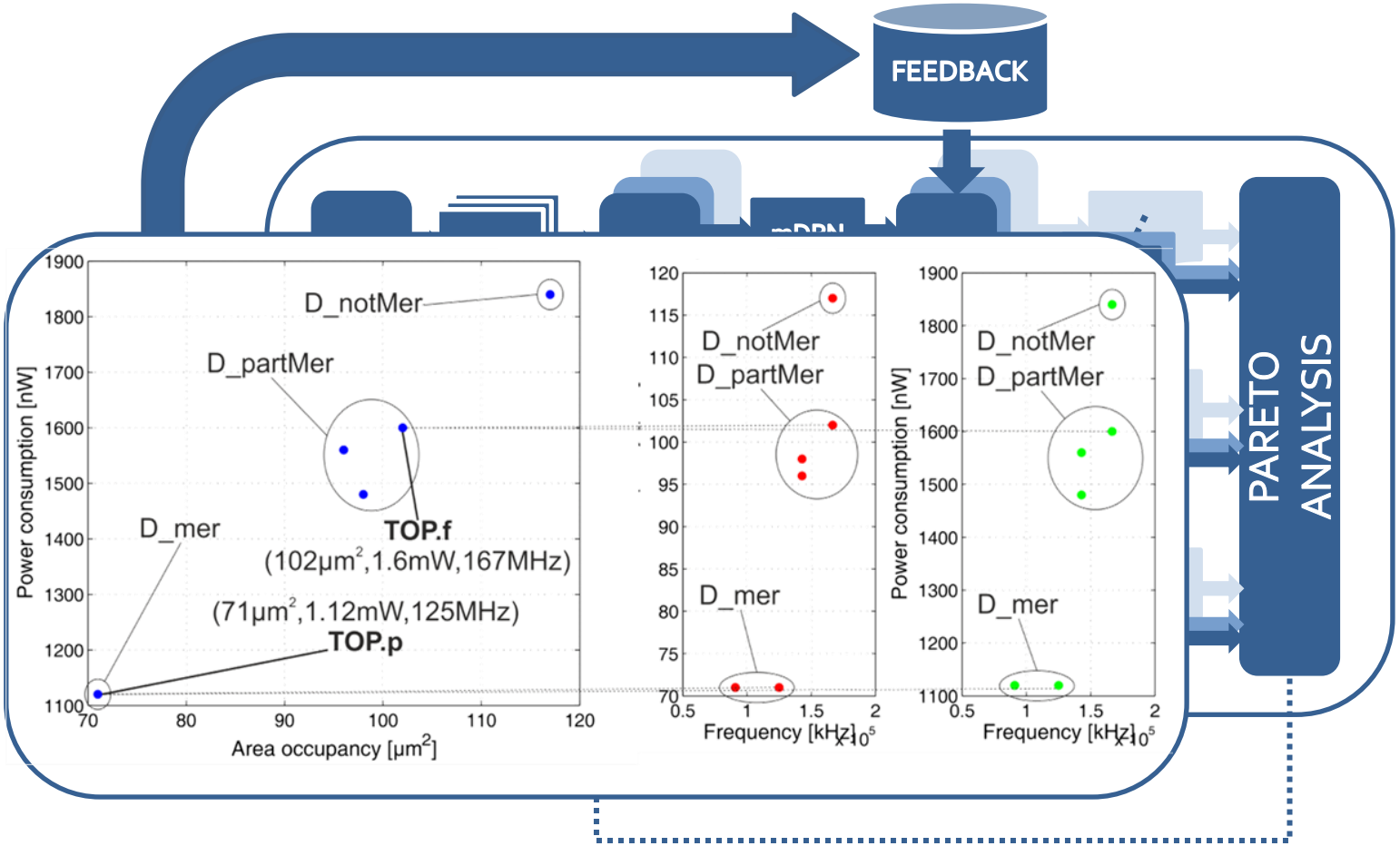

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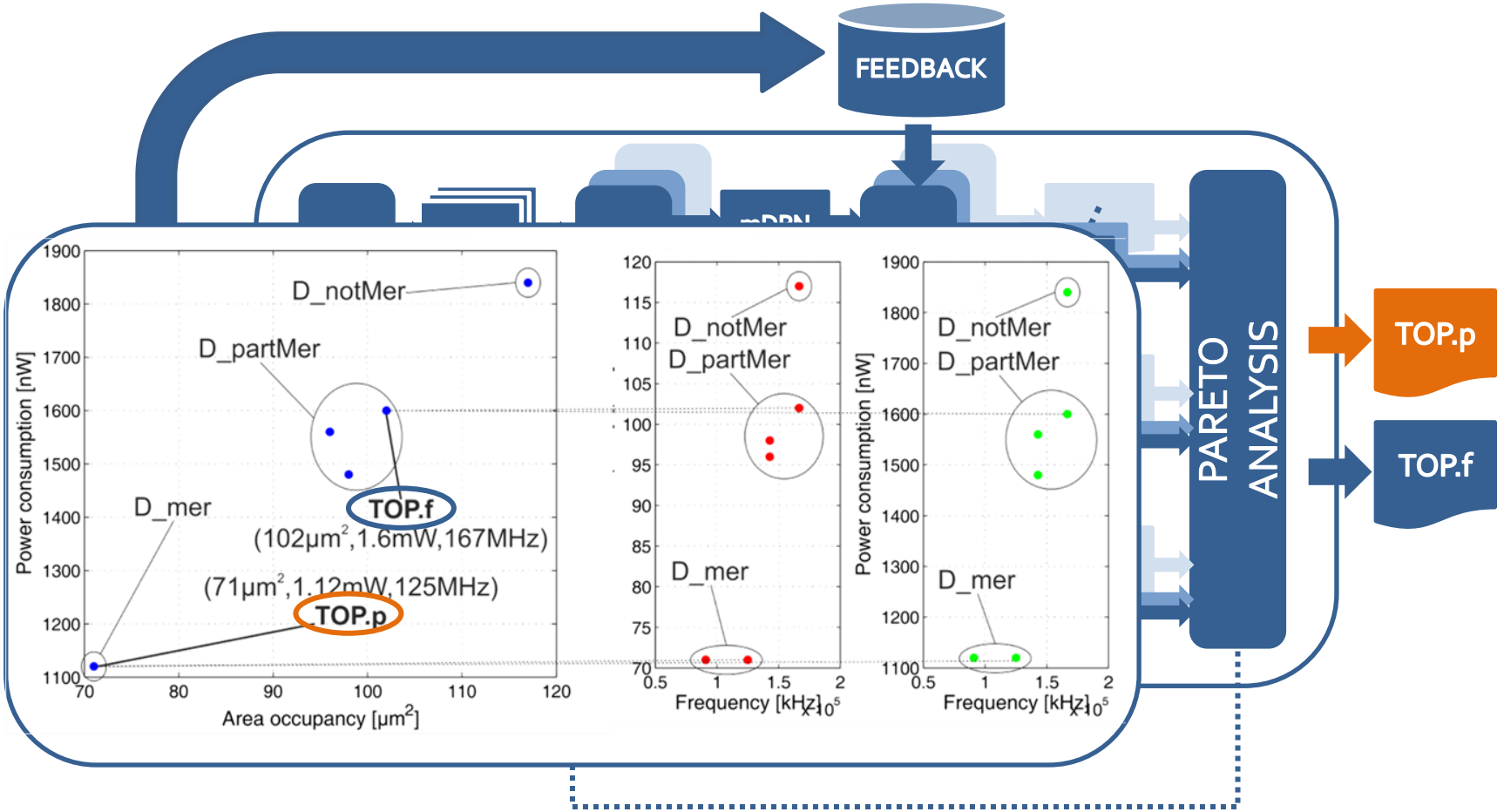

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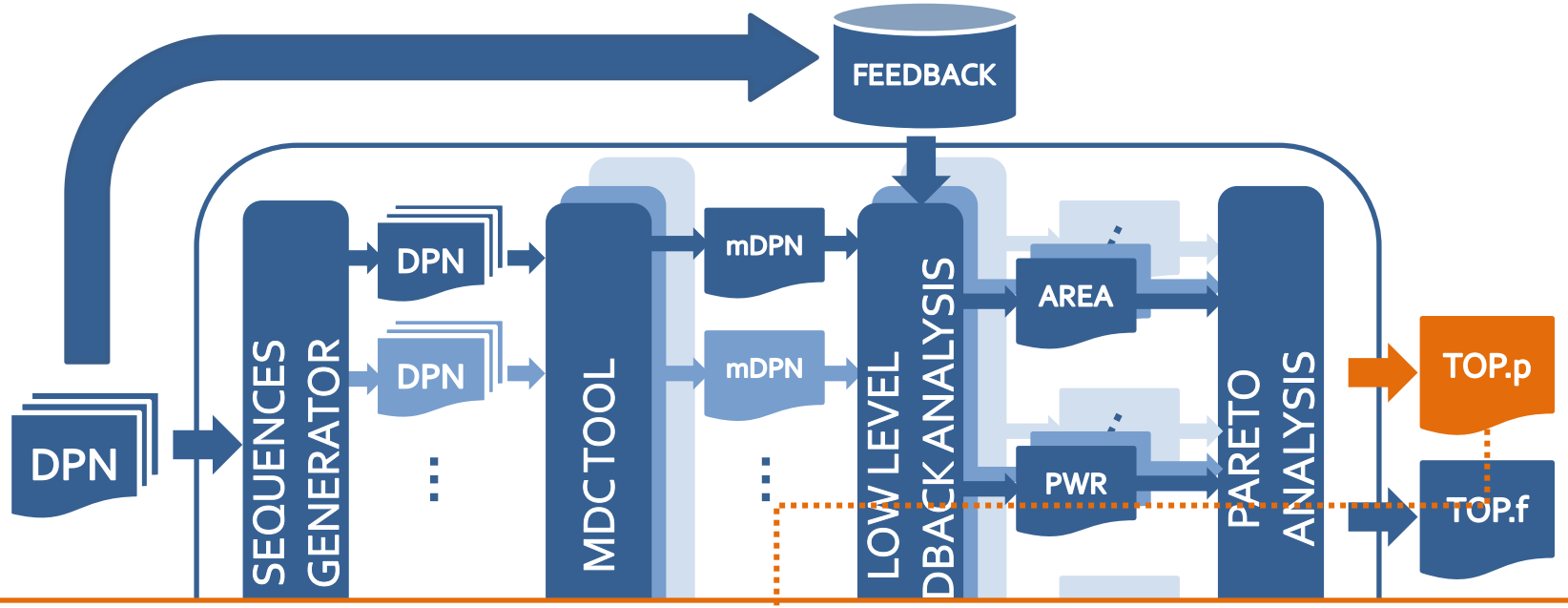
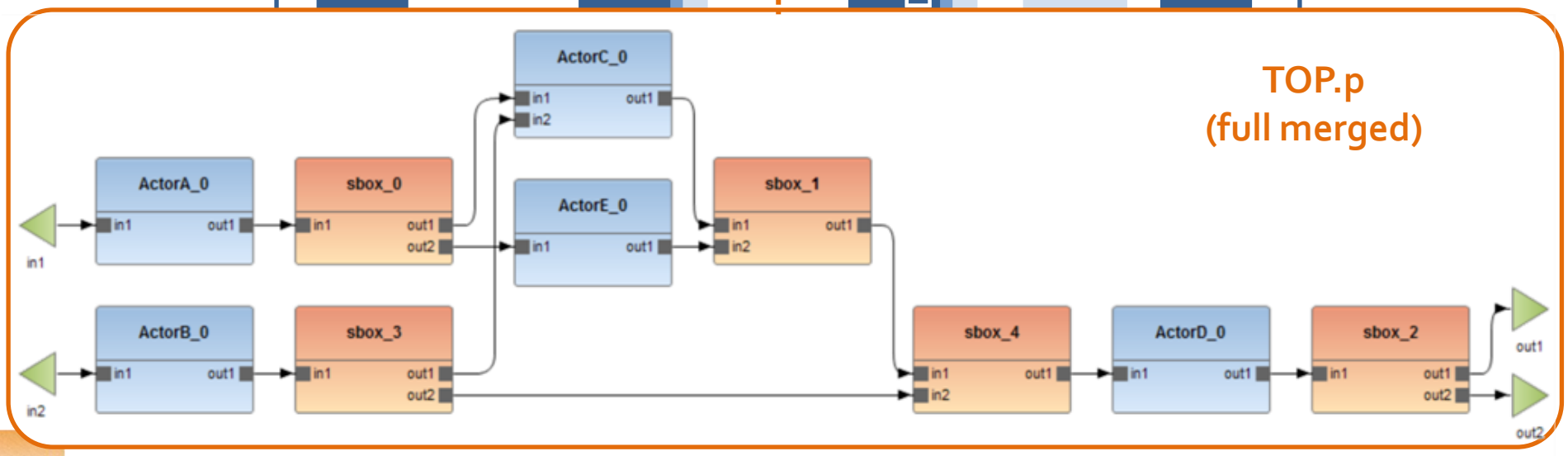
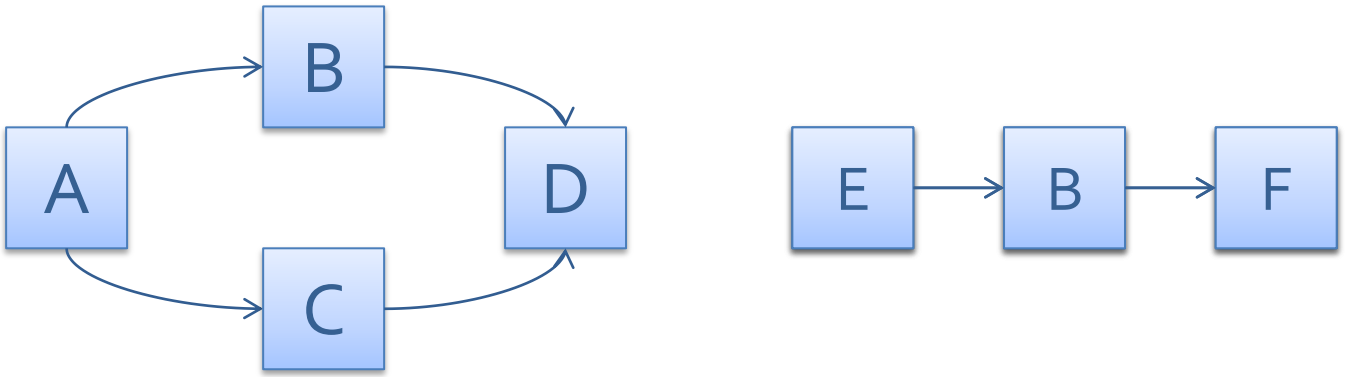
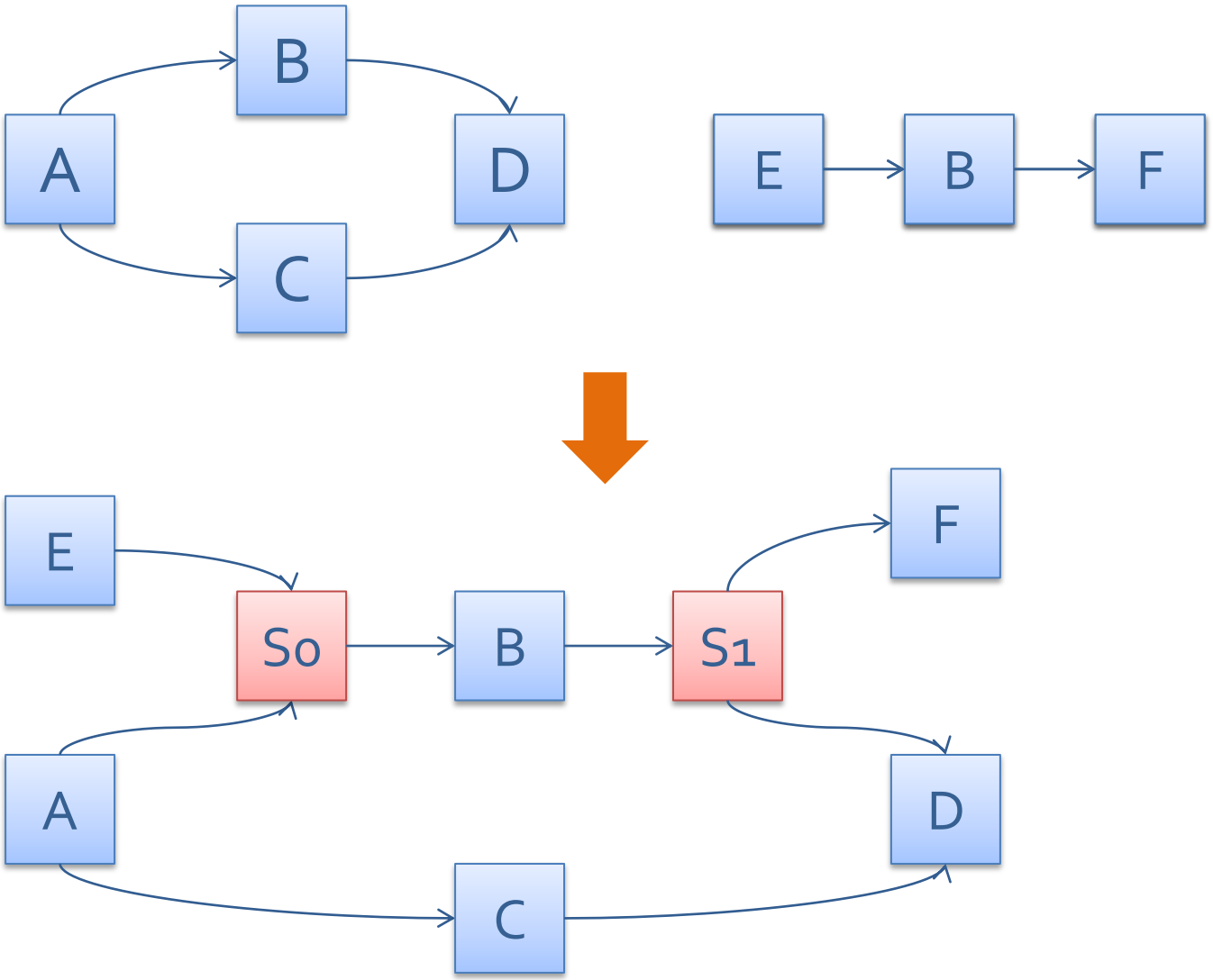




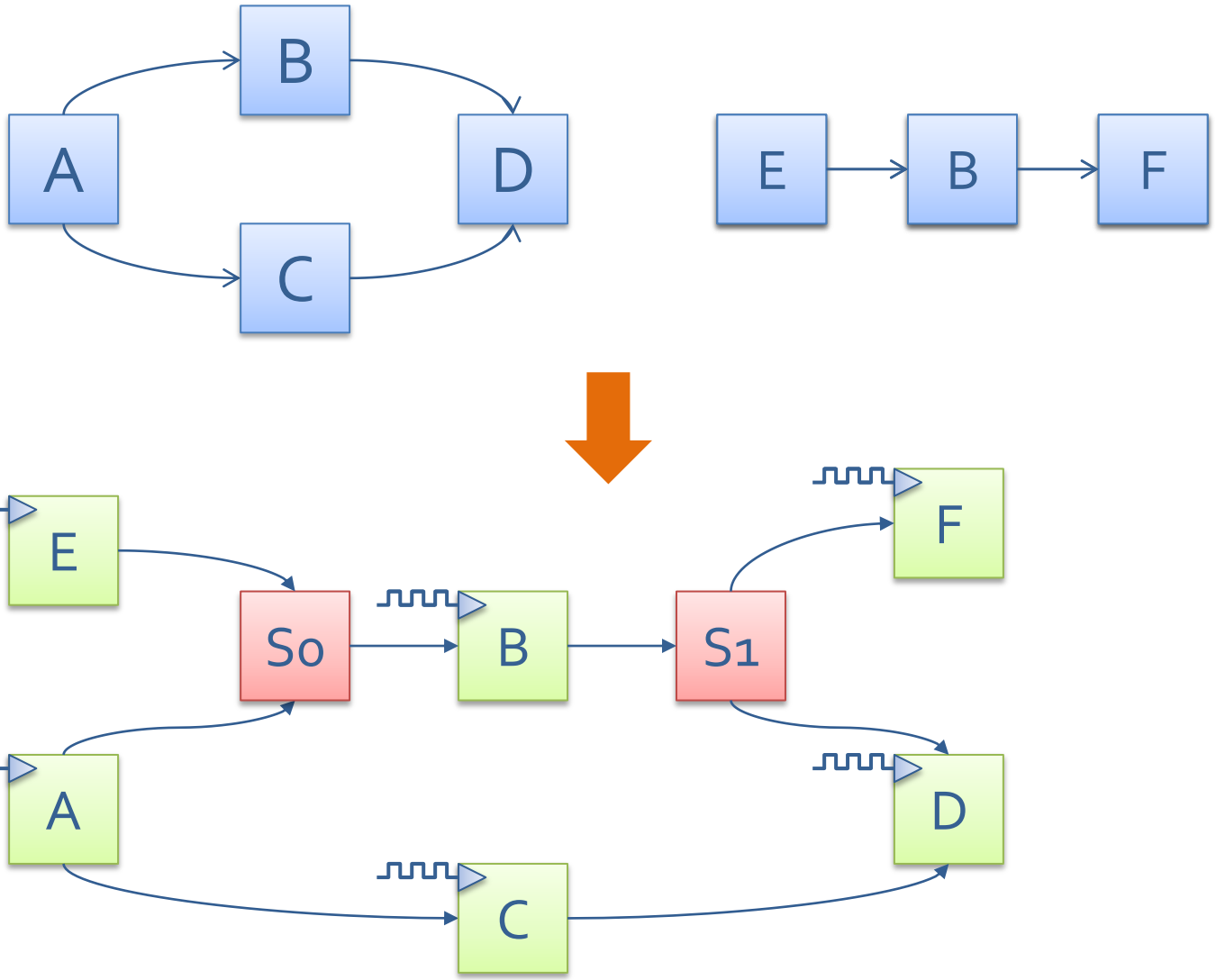
DYNAMIC POWER MANAGEMENT: BEHAVIORAL OPTIMIZATION



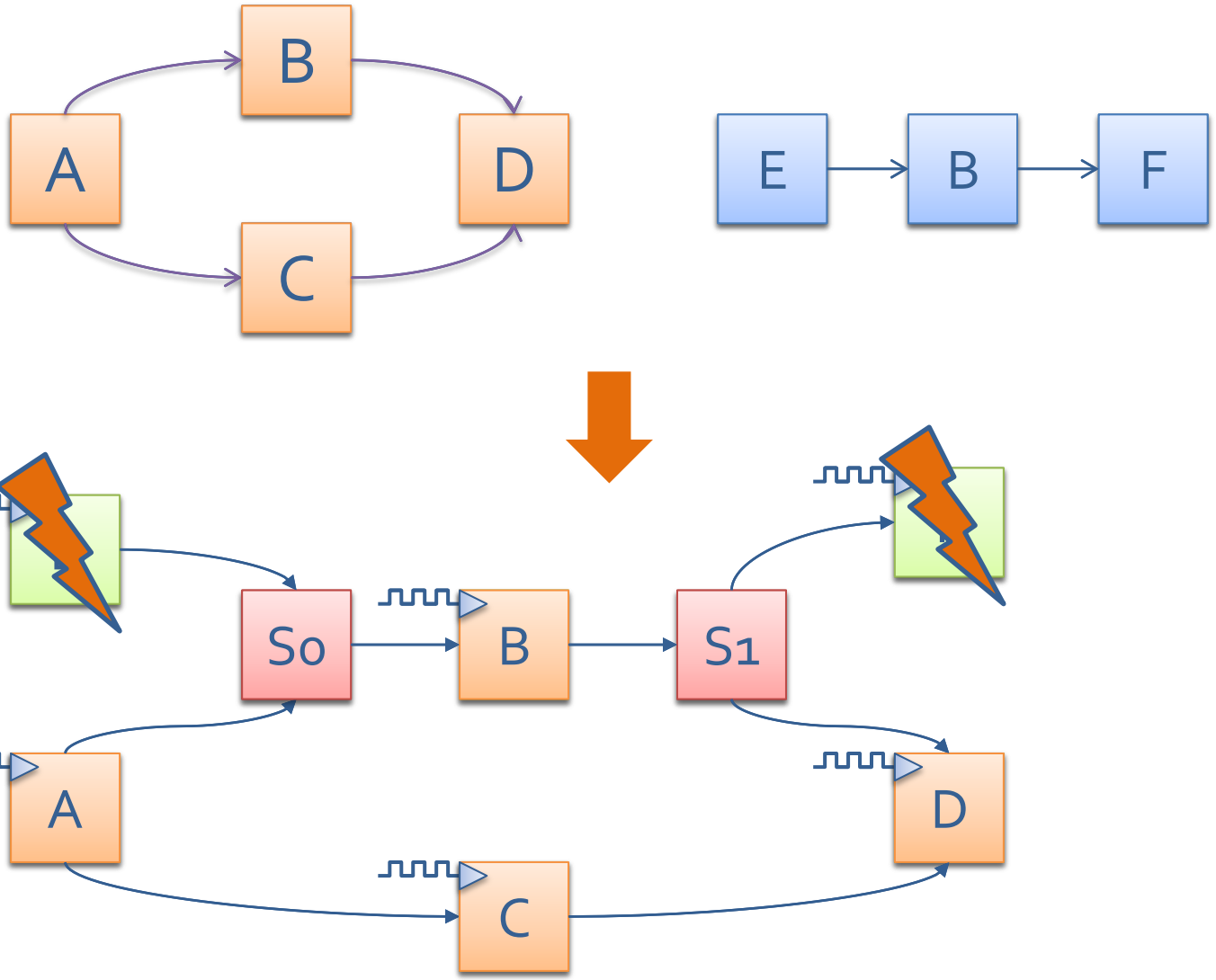
DYNAMIC POWER MANAGEMENT: BEHAVIORAL OPTIMIZATION



DYNAMIC POWER MANAGEMENT: BEHAVIORAL OPTIMIZATION



DYNAMIC POWER MANAGEMENT: BEHAVIORAL OPTIMIZATION



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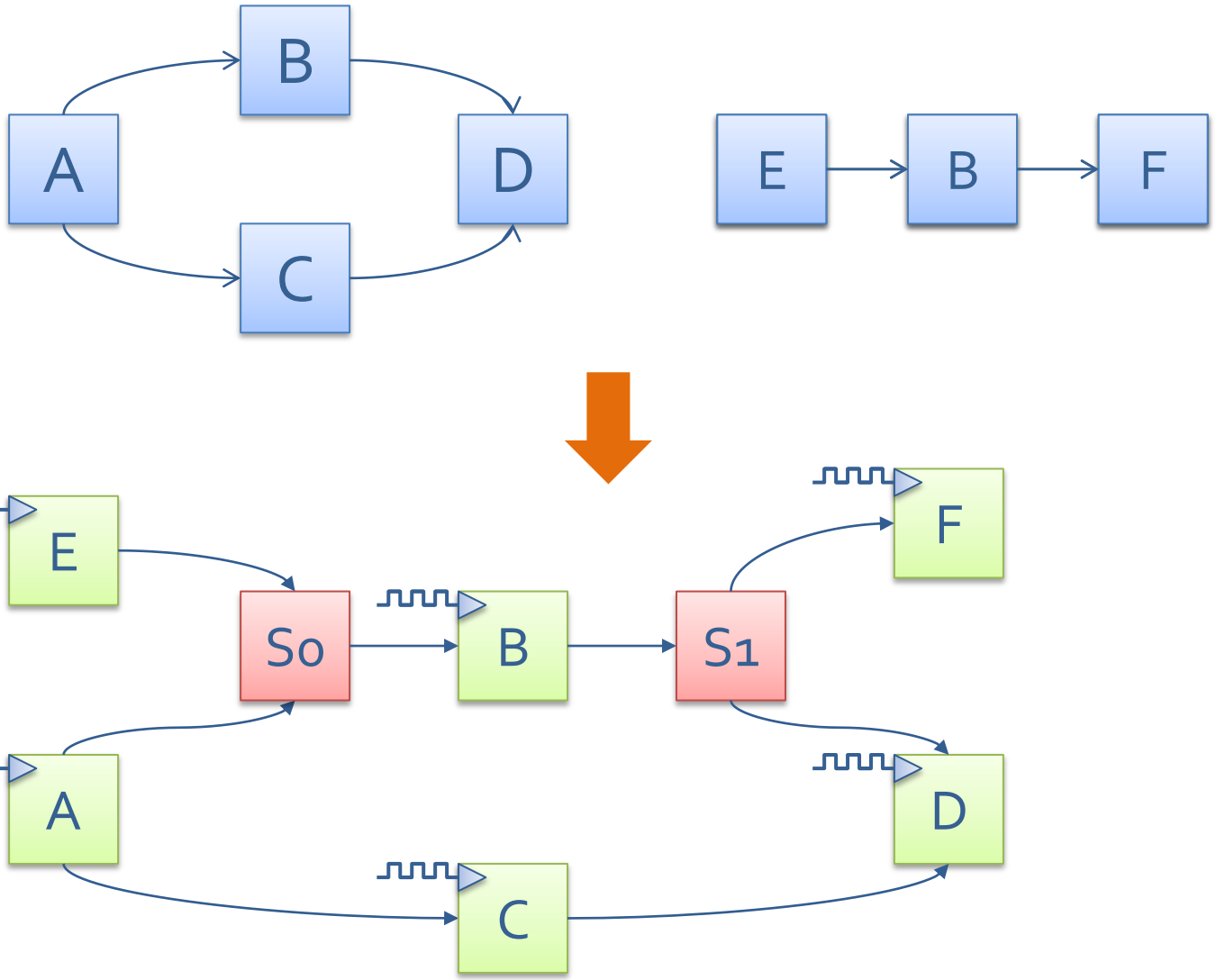

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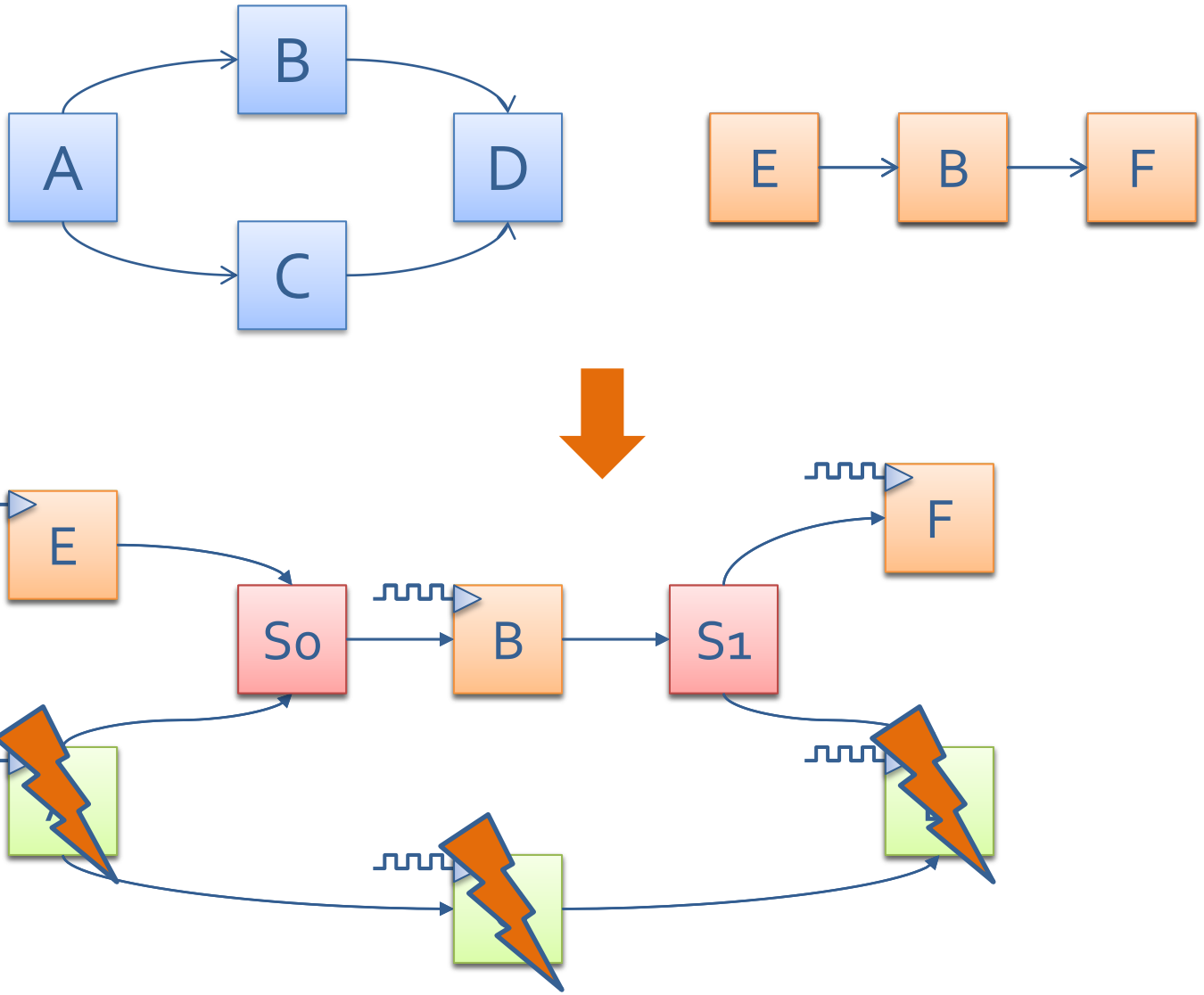

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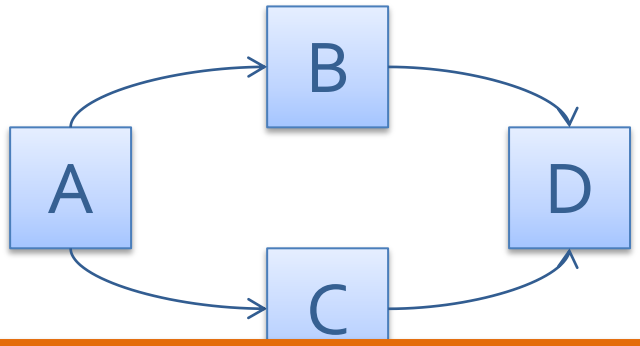
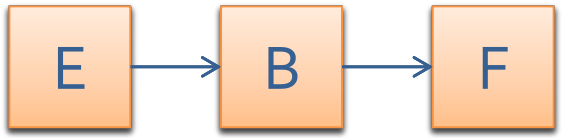
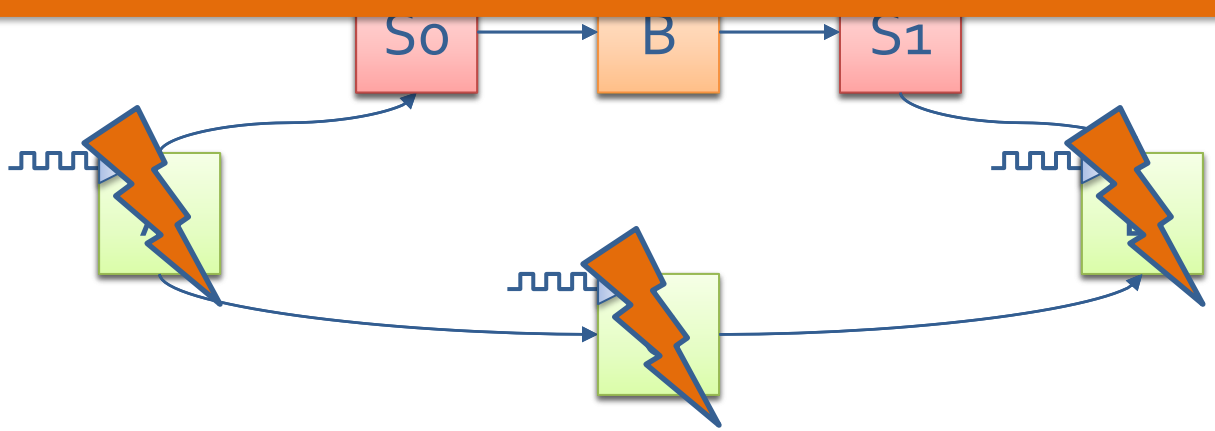
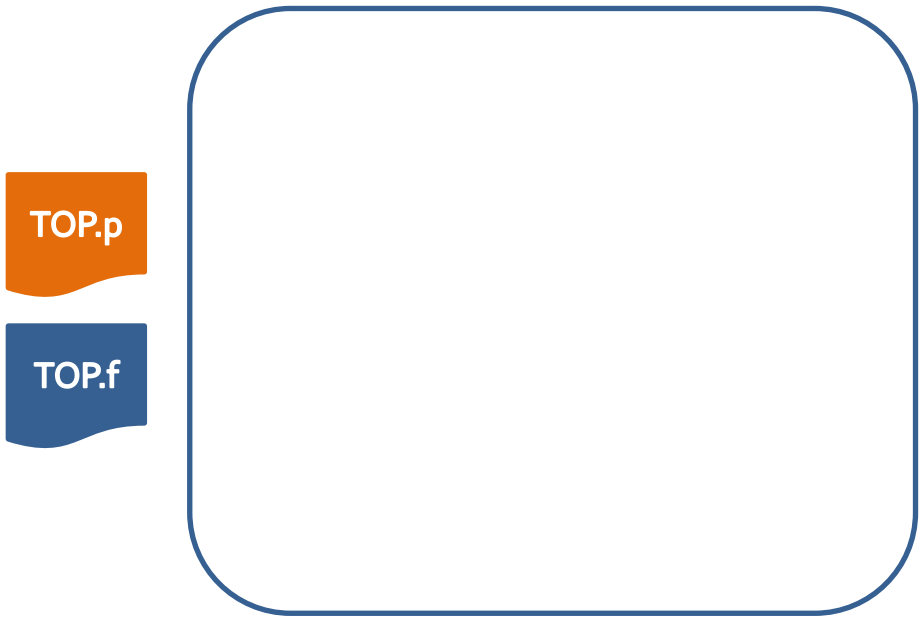




POWER WASTING due to the **RESOURCES** that are **NOT INVOLVED** in the current computation



DYNAMIC POWER MANAGEMENT: BEHAVIORAL OPTIMIZATION



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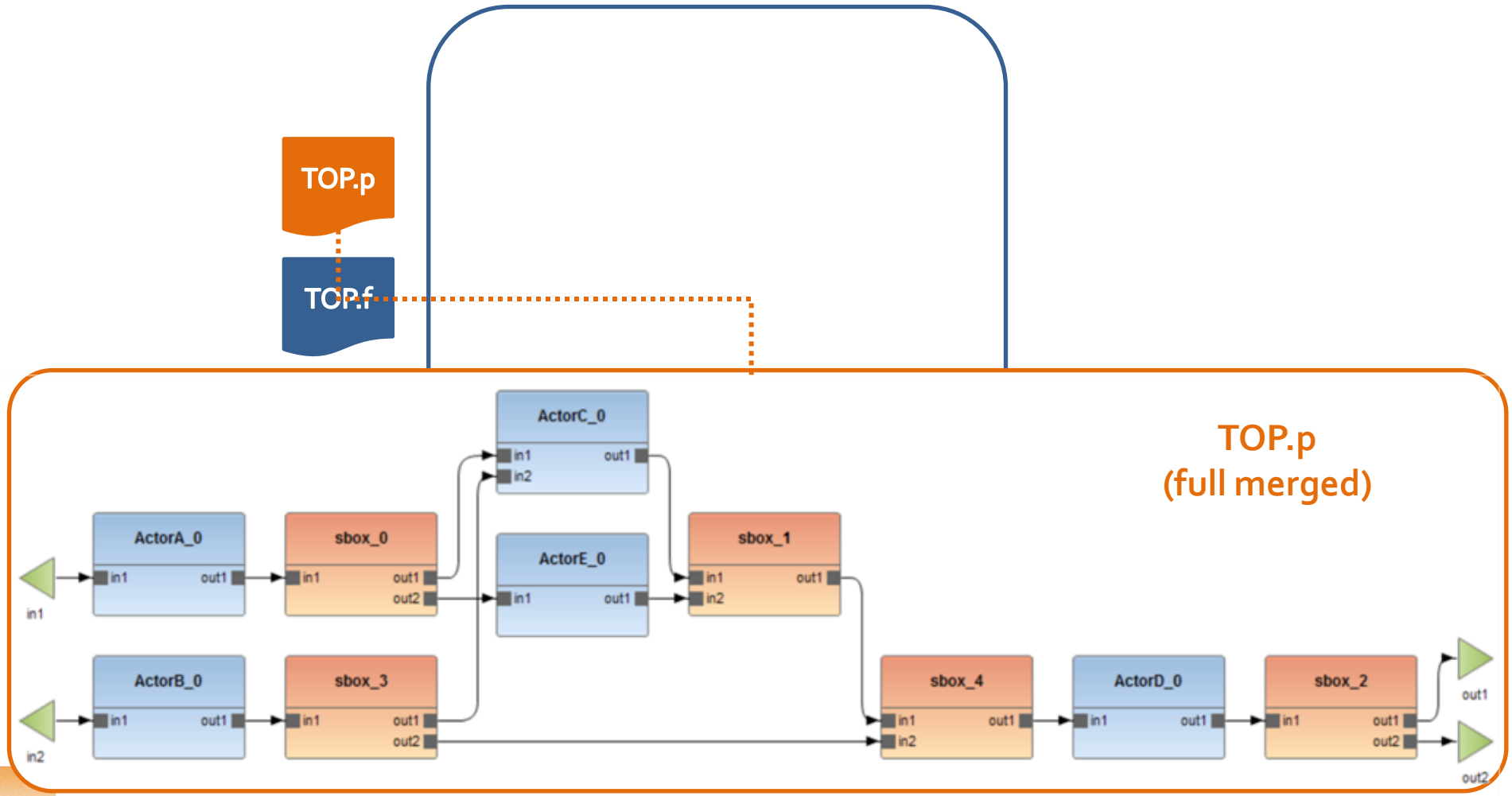

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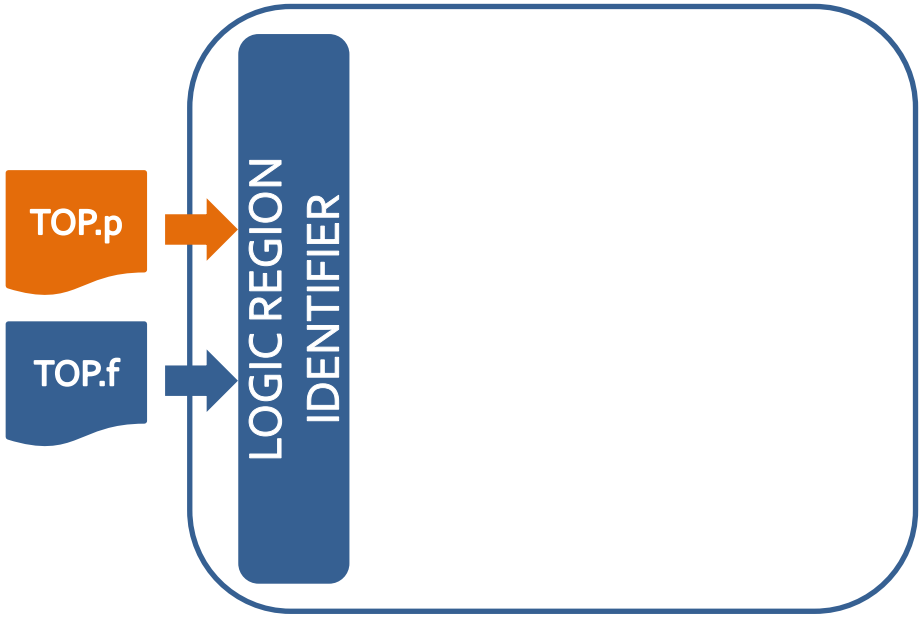

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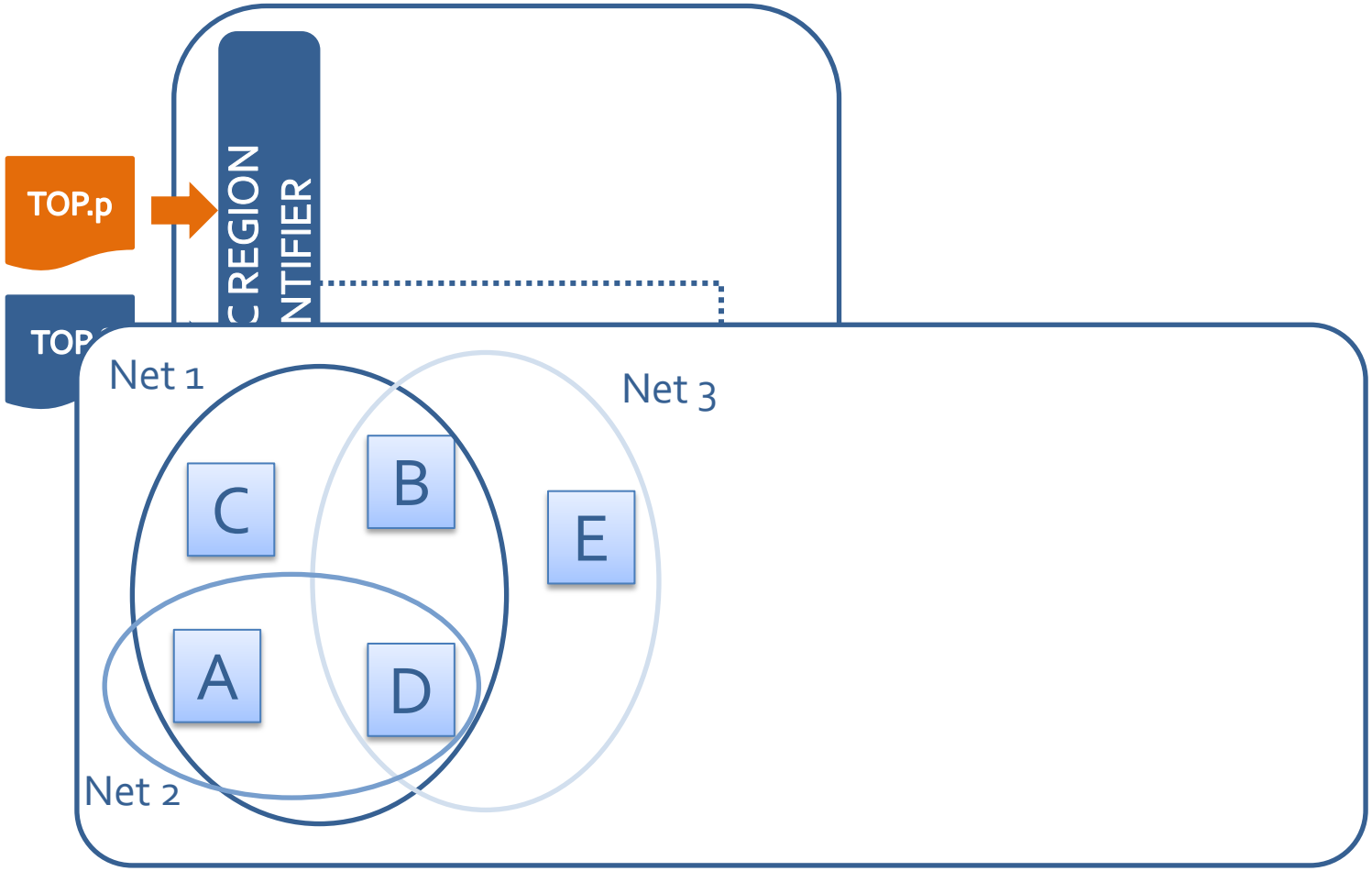

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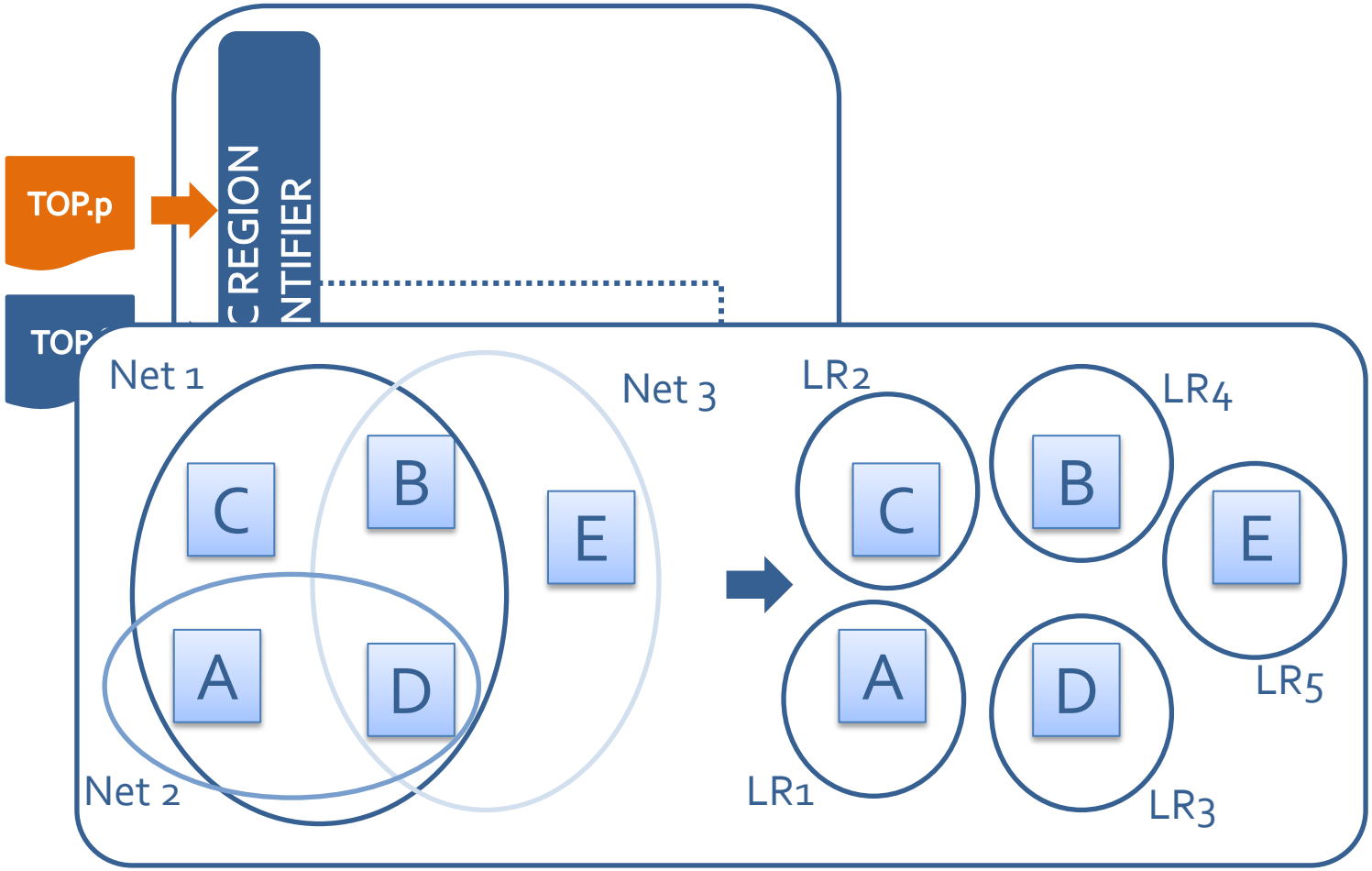

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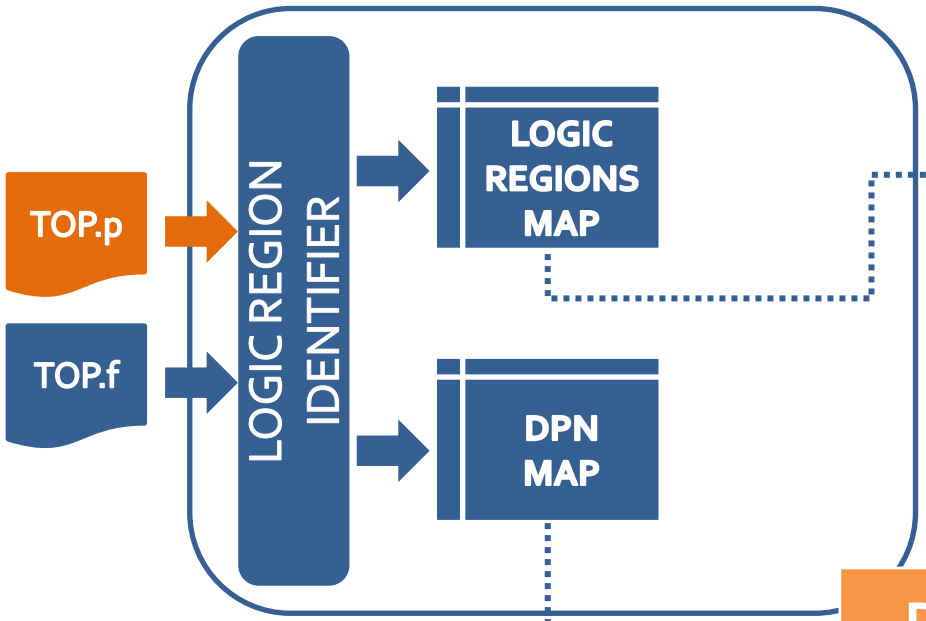
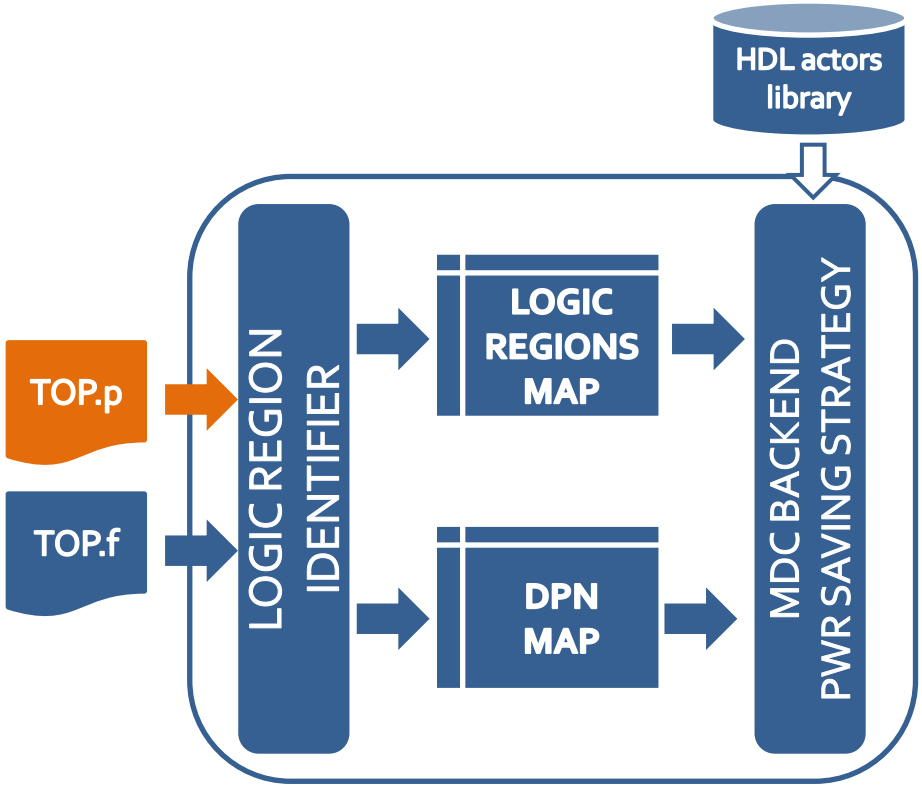


label	actors
LR1	A
LR2	C
LR3	D
LR4	B
LR5	E

DPN	regions
Net1	LR1,LR2,LR3,LR4
Net2	LR1,LR3
Net3	LR3,LR4,LR5

DYNAMIC POWER MANAGEMENT: BEHAVIORAL OPTIMIZATION



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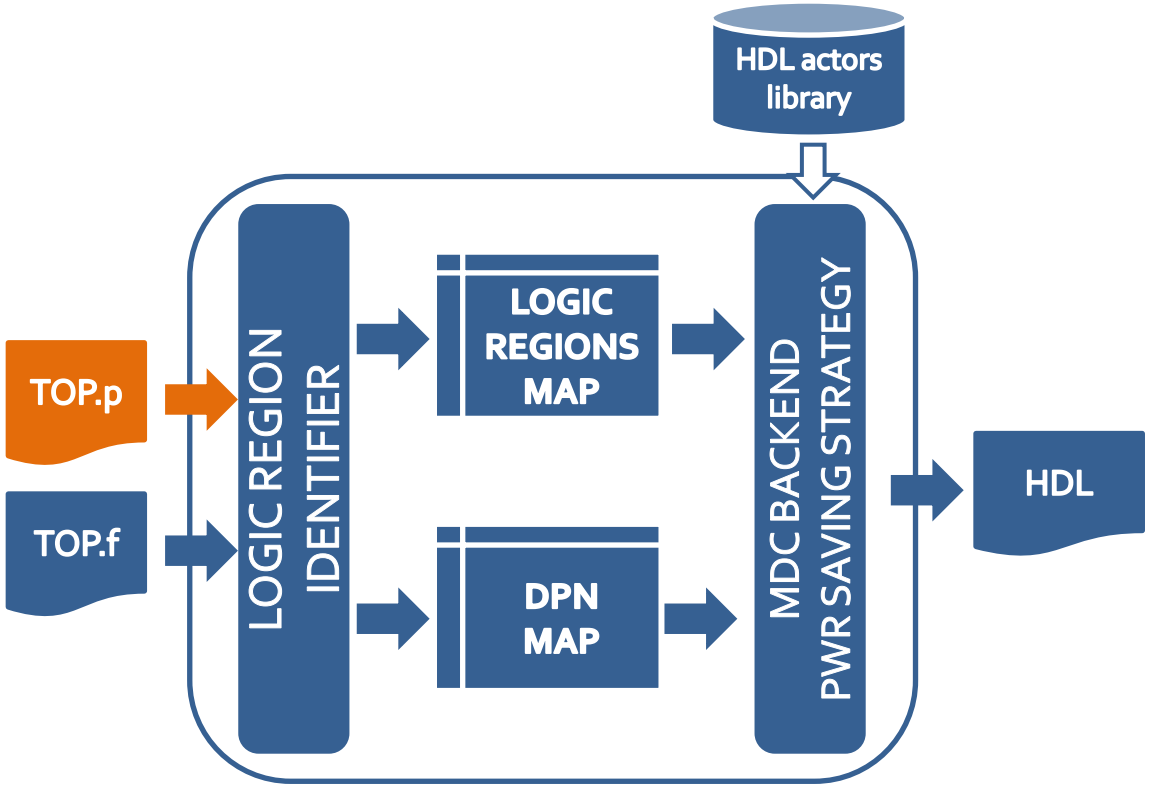

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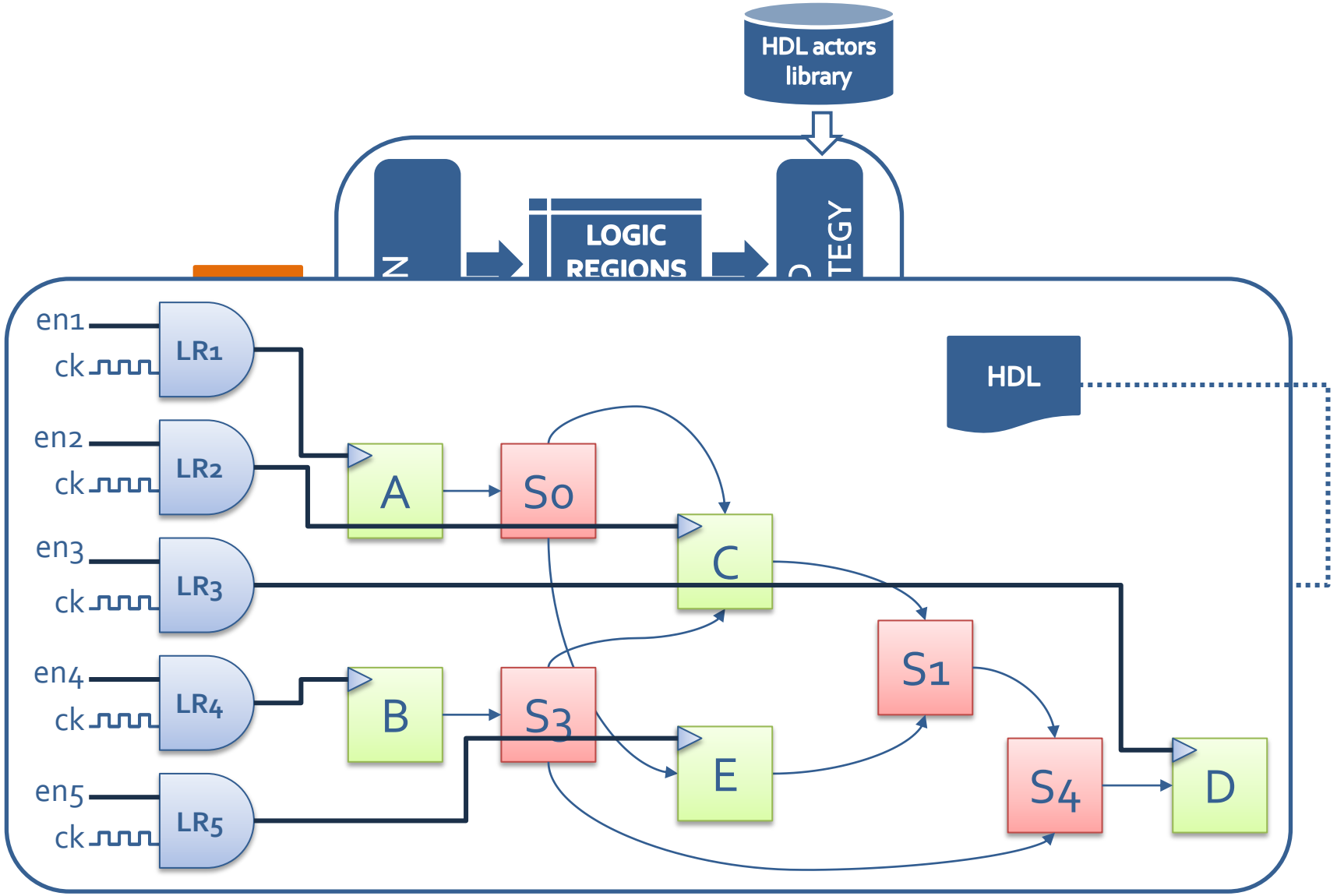

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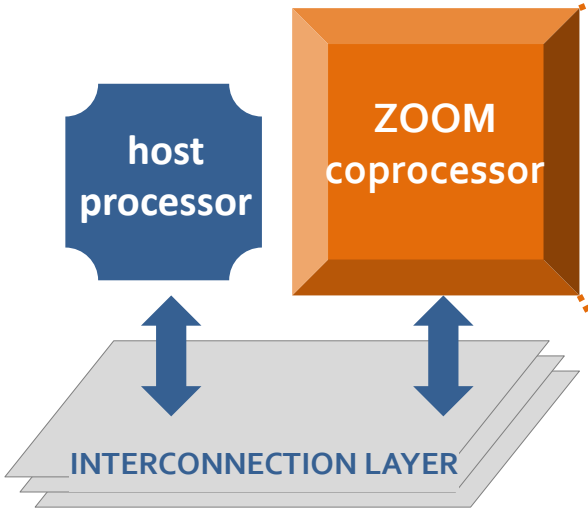
DESIGN UNDER TEST

APPLICATION	# KERNEL	# ACTORS	# SBOXES
zoom	7	87	54



DPN	#ACTORS	#OCC
Min-Max	1	1050
Abs	1	3150
Sbwlabel	17	2722
Median	9	1069
Check_GeneralBilevel	7	3072
Cubic	10	1070
Cubic_Conv	6	408

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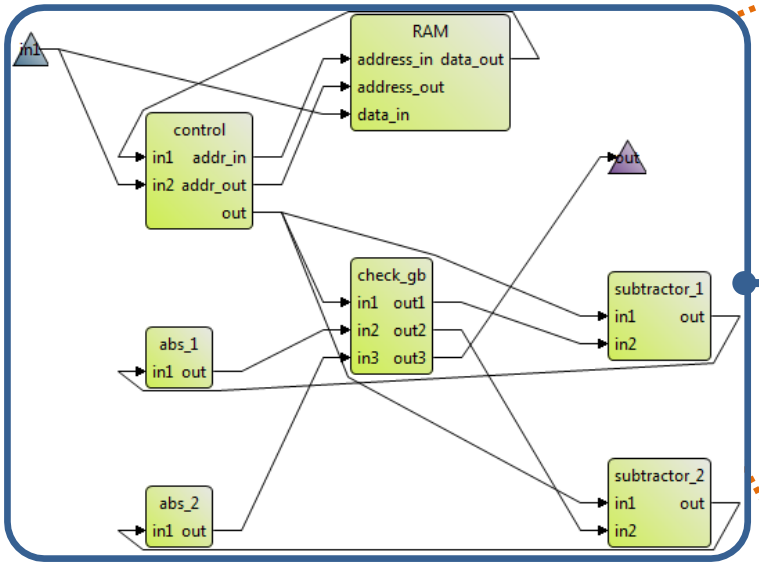

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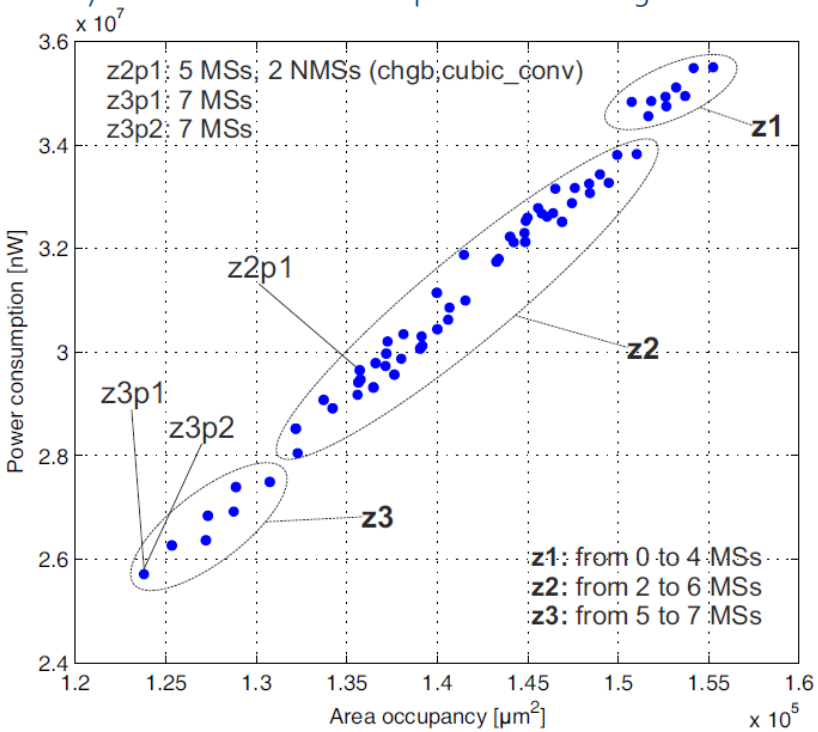
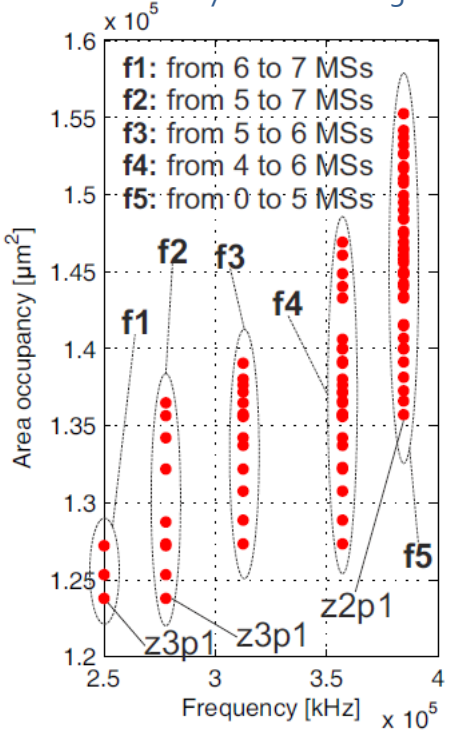
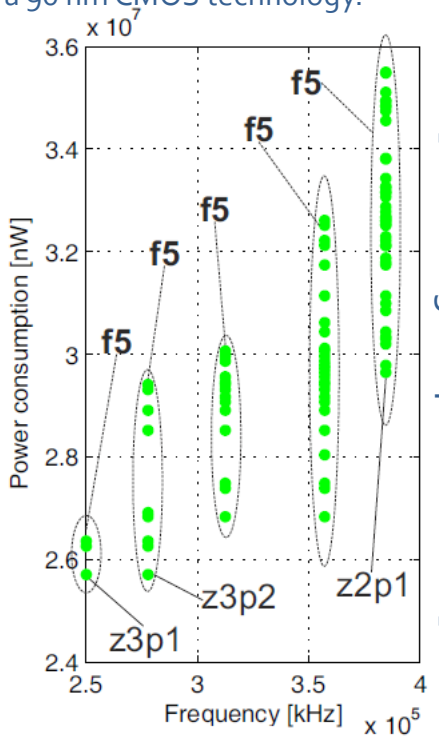
STRUCTURAL EVALUATION

Synthesis trials have been performed through the Cadence SOC Encounter synthesizer targeting a 90 nm CMOS technology.







[MS: Merged Specifications]

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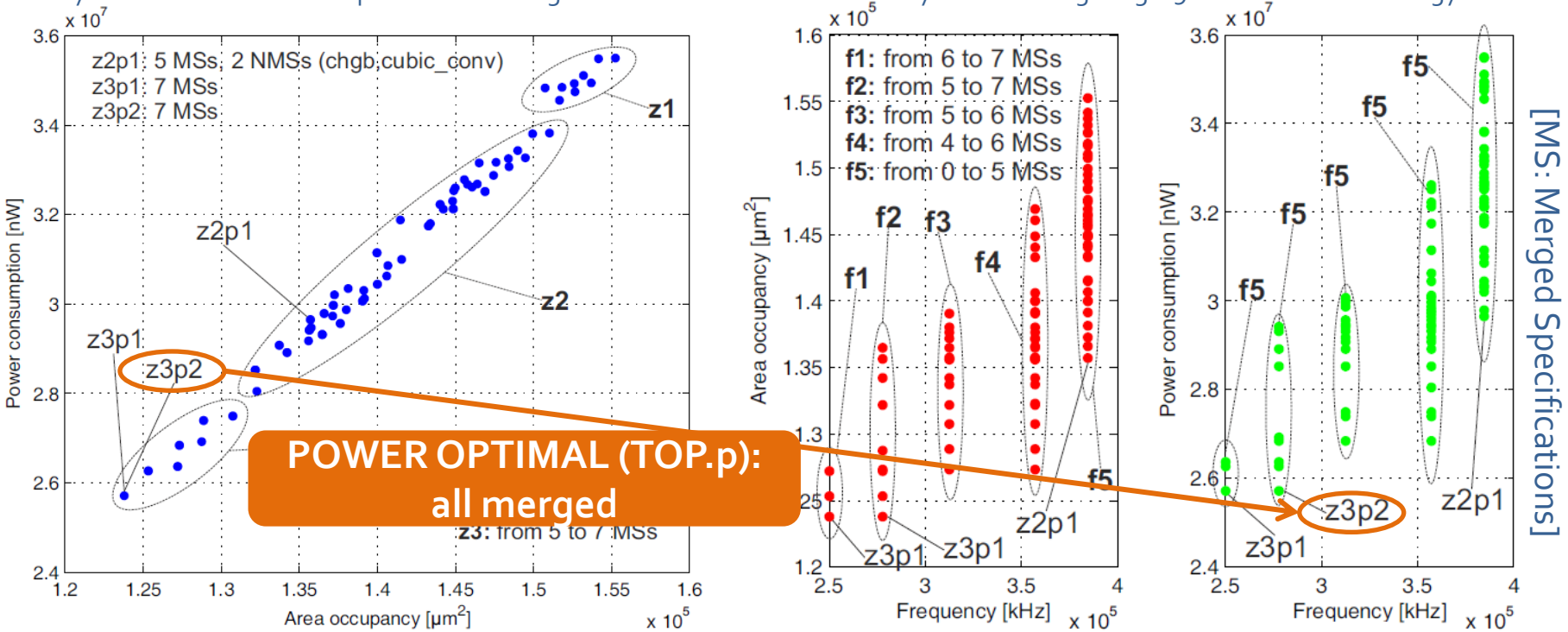

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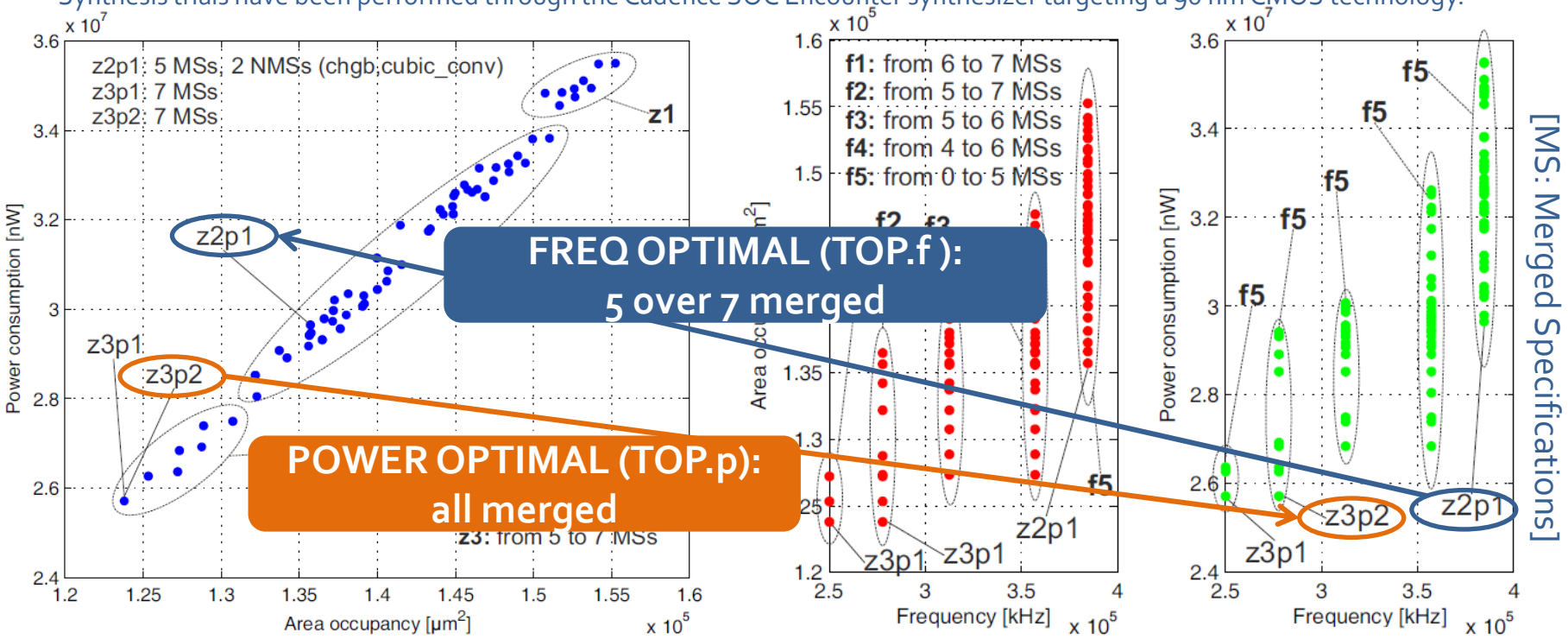

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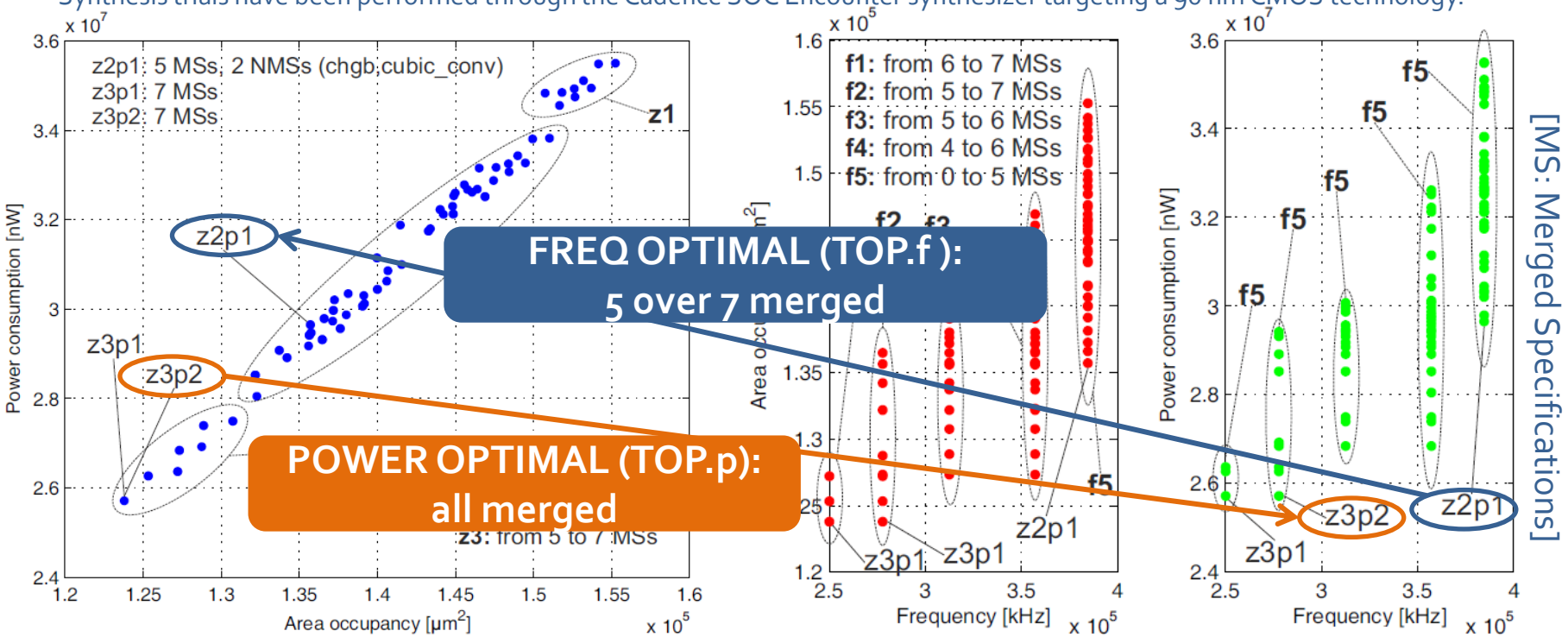

DESIGN	STATIC POWER ESTIMATION [mW]	STATIC POWER MEASURE [mW]	ESTIMATION ERROR
TOP.f	30.175	29.650	1.77%
TOP.p	25.833	25.716	0.45%
TOP.p vs TOP.f	-13.75%	-14.39%	7.78%

BEHAVIORAL EVALUATION

Synthesis trials have been performed through the Cadence SOC Encounter synthesizer targeting a 90 nm CMOS technology.

DESIGN	# of LRs	NOCG AREA [µm2]	CG AREA [µm2]	CG vs NOCG
TOP.f	9	135819	136076	+0.19%
TOP.p	13	124026	124579	+0.25%
TOP.p vs TOP.f	+44.44%	-8.68%	-8.45%	+31.58%

NOCG = without clock gating implementation
AUTO = with the synthesizer automatic register-level clock gating implementation
CG = with the proposed high-level clock gating implementation

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DESIGN	DYNAMIC POWER	
	CG vs NOCG	CG vs AUTO
TOP.f	-74.86%	-69.06%
TOP.p	-71.30%	-63.75%
TOP.p vs TOP.f	-13.75%	-14.39%

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- Future developments
  - Power gating on different logic regions
  - Improvements in the estimation models
  - Heuristic for the profiler design space exploration

ACKNOWLEDGEMENTS

The research leading to these results has received funding from:

- the Region of Sardinia L.R.7/2007 under grant agreement CRP-18324 [RPCT Project].

- the Region of Sardinia, Young Researchers Grant, POR Sardegna FSE 2007-2013, L.R.7/2007 "Promotion of the scientific research and technological innovation in Sardinia"

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SIPS 2014

Carlo Sau
Università degli Studi di Cagliari
DIEE – Dept. of Electrical and Electronics Eng.
EOLAB - Microelectronics and Bioeng. Lab.

Power-Awareness in Coarse-Grained Reconfigurable Designs: a Dataflow Based Strategy

QUESTIONS