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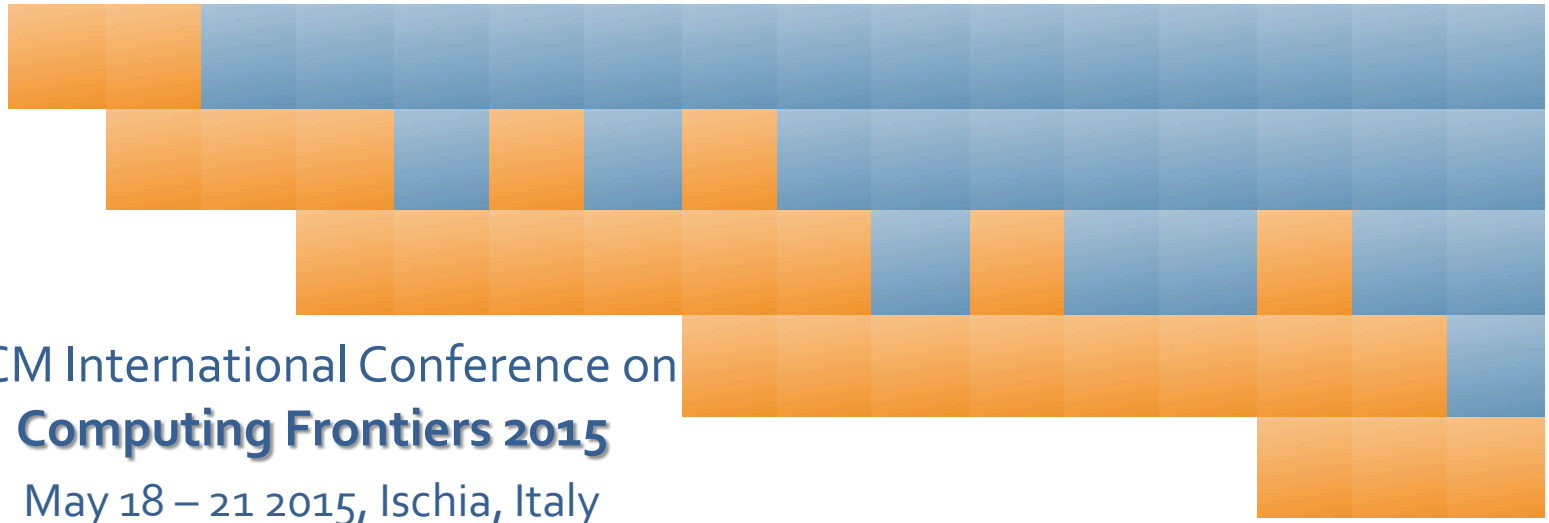
EOLAB - Microelectronics and Bioeng. Lab.

Francesca Palumbo
Università degli Studi di Sassari
PolComIng
Information Engineering Unit

Automated Power Gating Methodology for Dataflow-Based Reconfigurable Systems



ACM International Conference on
Computing Frontiers 2015
May 18 – 21 2015, Ischia, Italy

Outline

- Introduction
  - Increasing Complexity
  - Problem Statement
- Background
  - Dataflow Model of Computation
  - Coarse-Graine Reconfiguration: Multi-Dataflow Composer Tool - MDC
  - Power Management
- Automated Power Gating Strategy
  - Logic Regions Identification
  - Power Gating Implementation
- Performance Assessment
  - Design Under Test
  - Experimental Results
- Final Remarks and Future Directions

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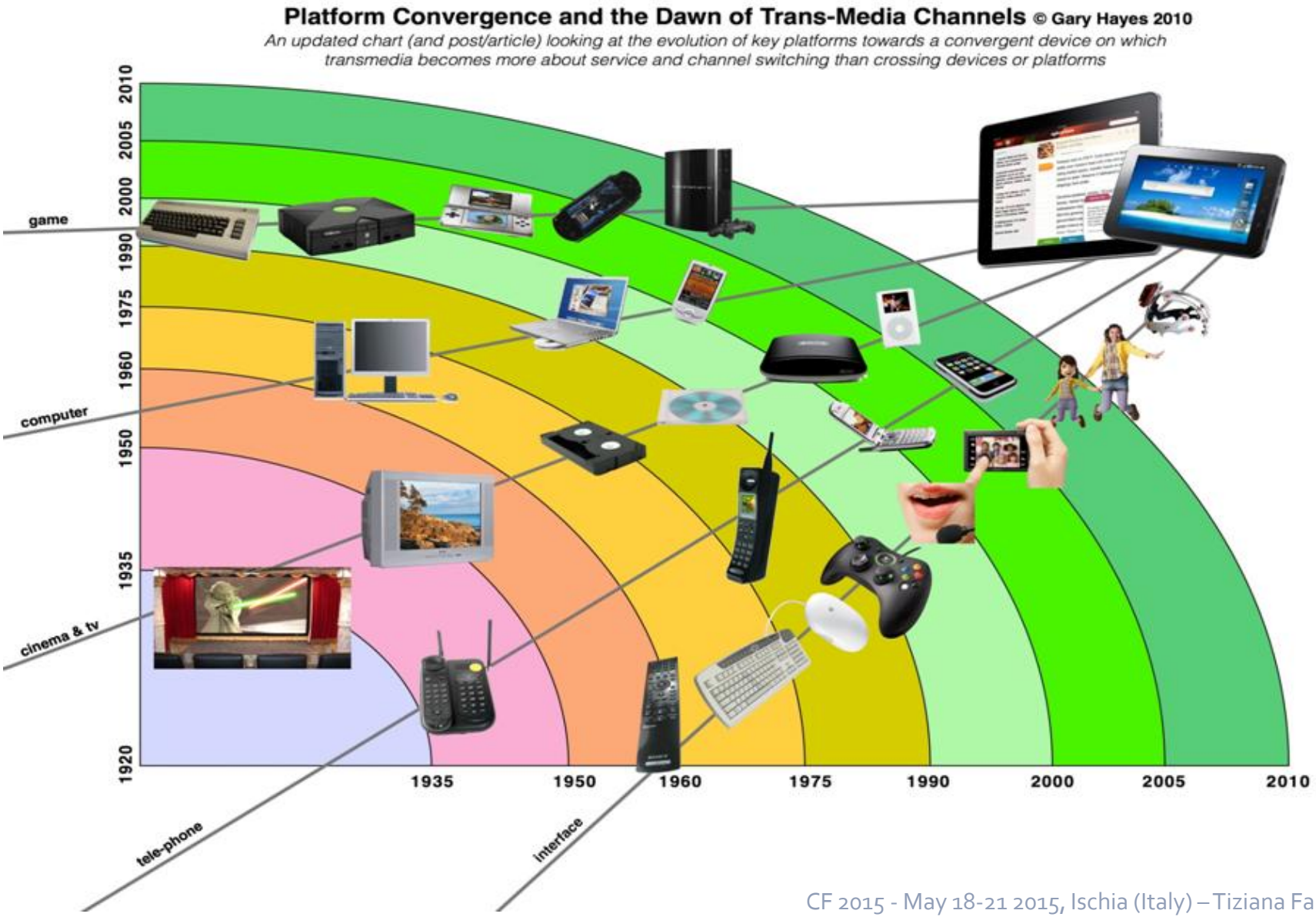
Introduction

Increasing Complexity



Introduction

Increasing Complexity

10 years ago => 1 h battery life

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MP3 player: more songs than power-life ☹

Introduction

Problem Statement

Consumers need:

- Integrated complex and fancy resurce-intensive applications
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Possible solutions:

- **Dataflow Model of Computation**
  - Modularity and parallelism → **INTEGRATION AND RE-USABILITY**
- **Coarse-graine reconfiguration**
  - Flexibility and resource sharing → **MULTI-APPLICATION PORTABLE DEVICES**

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- **Coarse-graine reconfiguration**
  - Flexibility and resource sharing → **MULTI-APPLICATION PORTABLE DEVICES**

Technology limitation:

- Battery technology is **not evolving fast enough**
  - Need to **MANAGE POWER CONSUMPTION**

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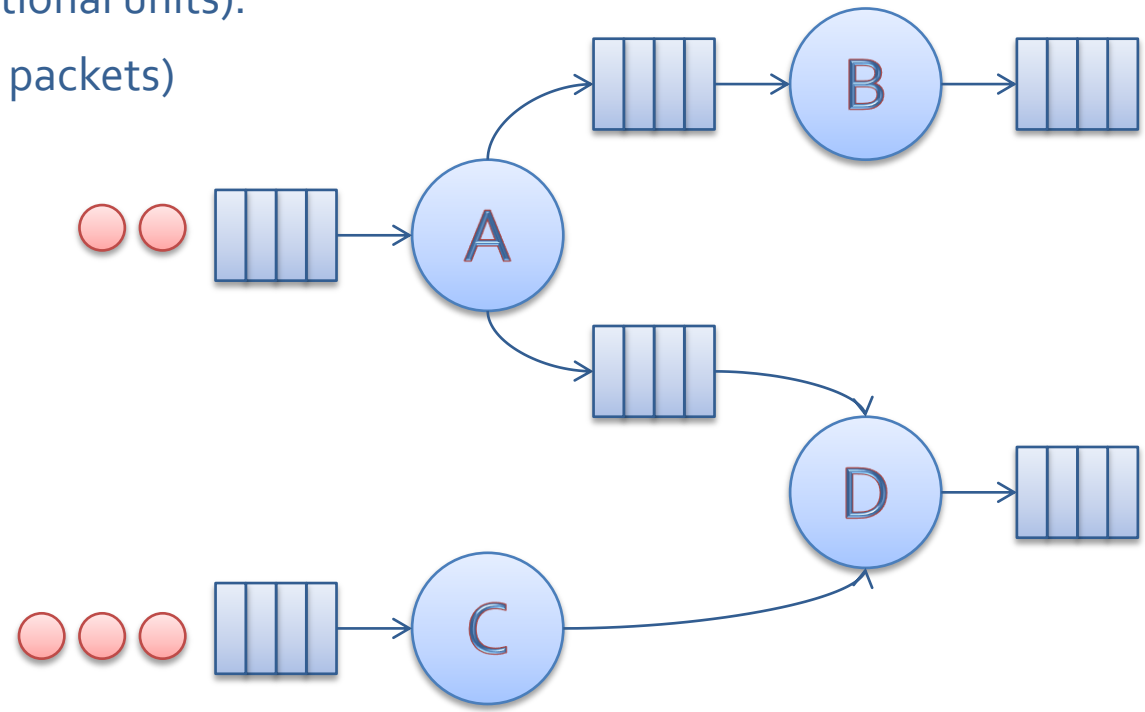
Dataflow Model of Computation

DATAFLOW FORMALISM

- Directed graph of **actors** (functional units).
- Actors exchange **tokens** (data packets) through dedicated channels

CHARATERISTICS

- Explicit the intrinsic application **parallelism**.
- **Modularity** favours model **re-usability/adaptivity.**



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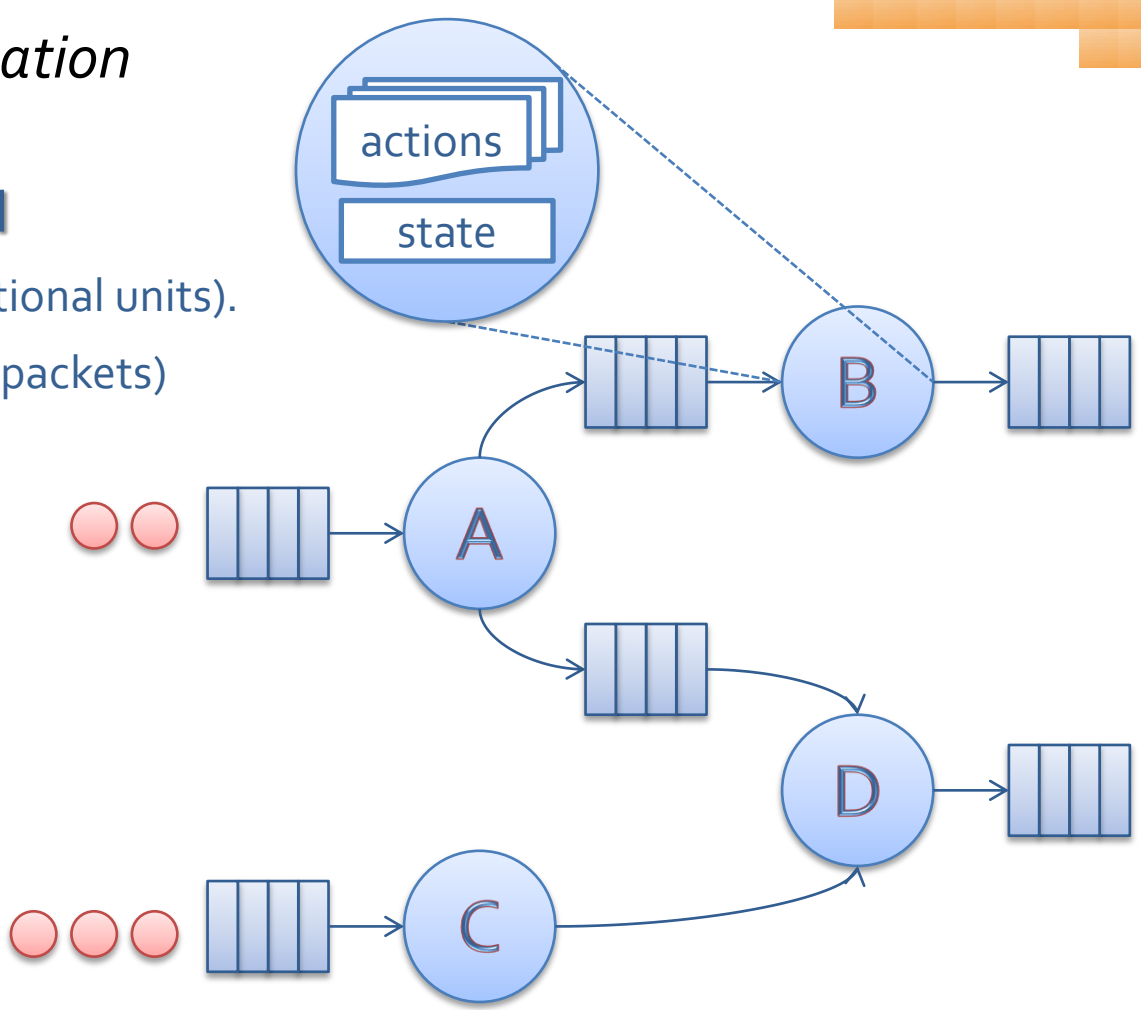

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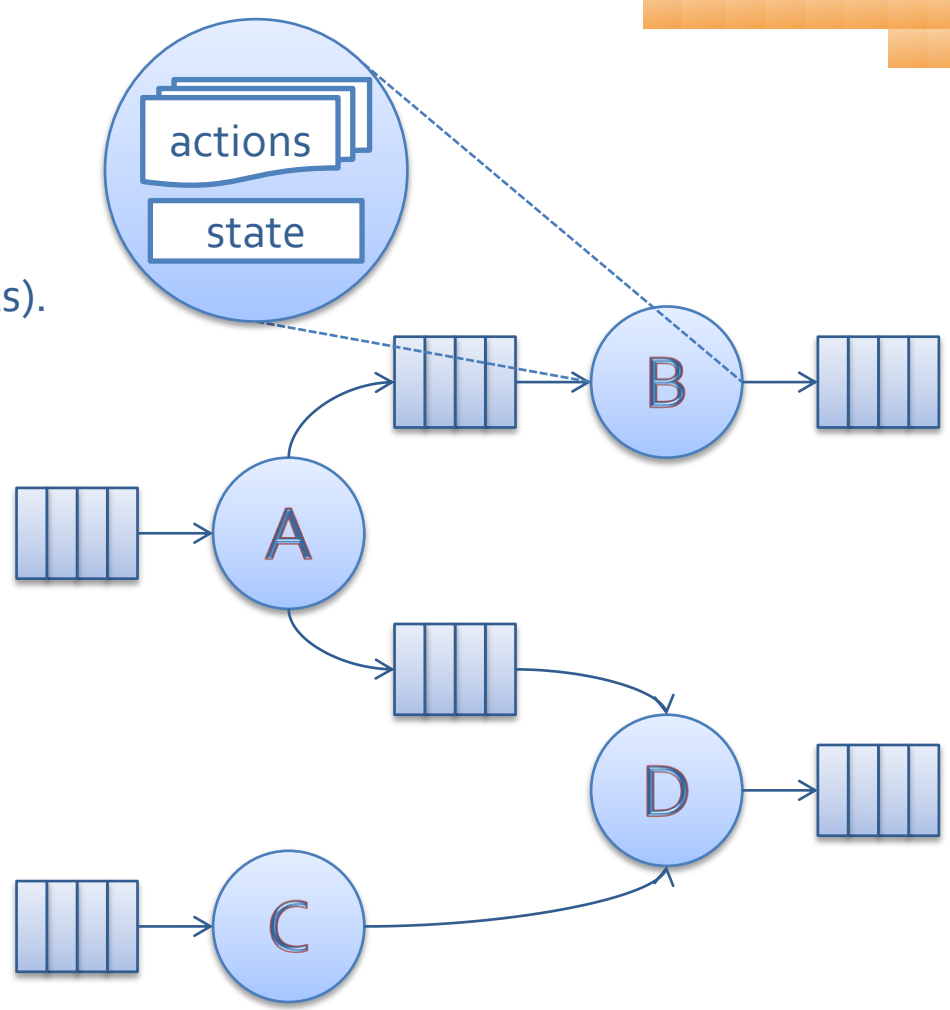

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MPEG RVC-CAL

- **ISO/IEC 23001-4 (or MPEG-B pt. 4)** [2009]: formalism definition.
- **ISO/IEC 23002-4 (or MPEG-C pt. 4)**[2010]: Video Tool Library.

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Coarse-Graine Reconfiguration: Multi-Dataflow Composer Tool - MDC

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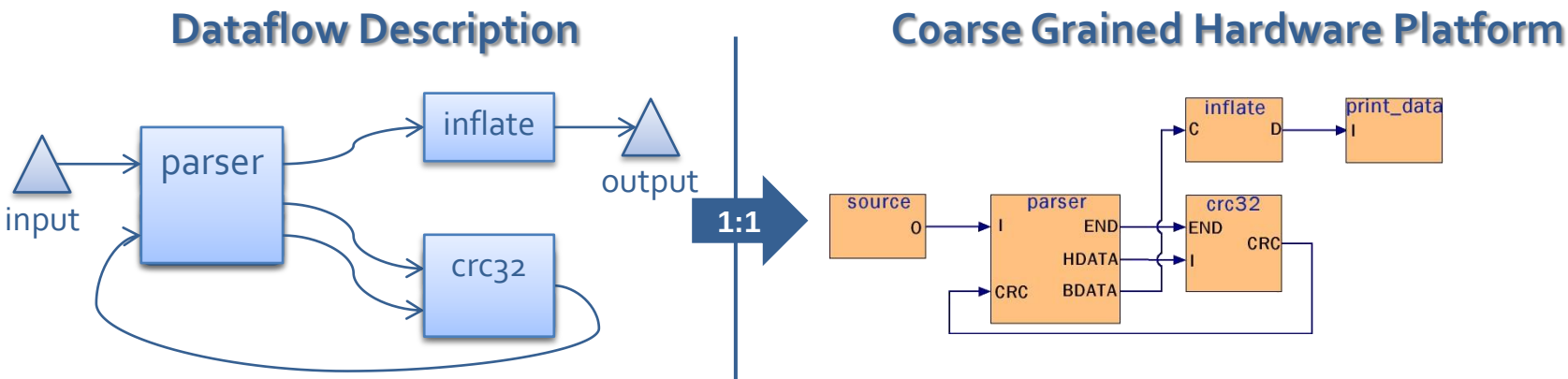

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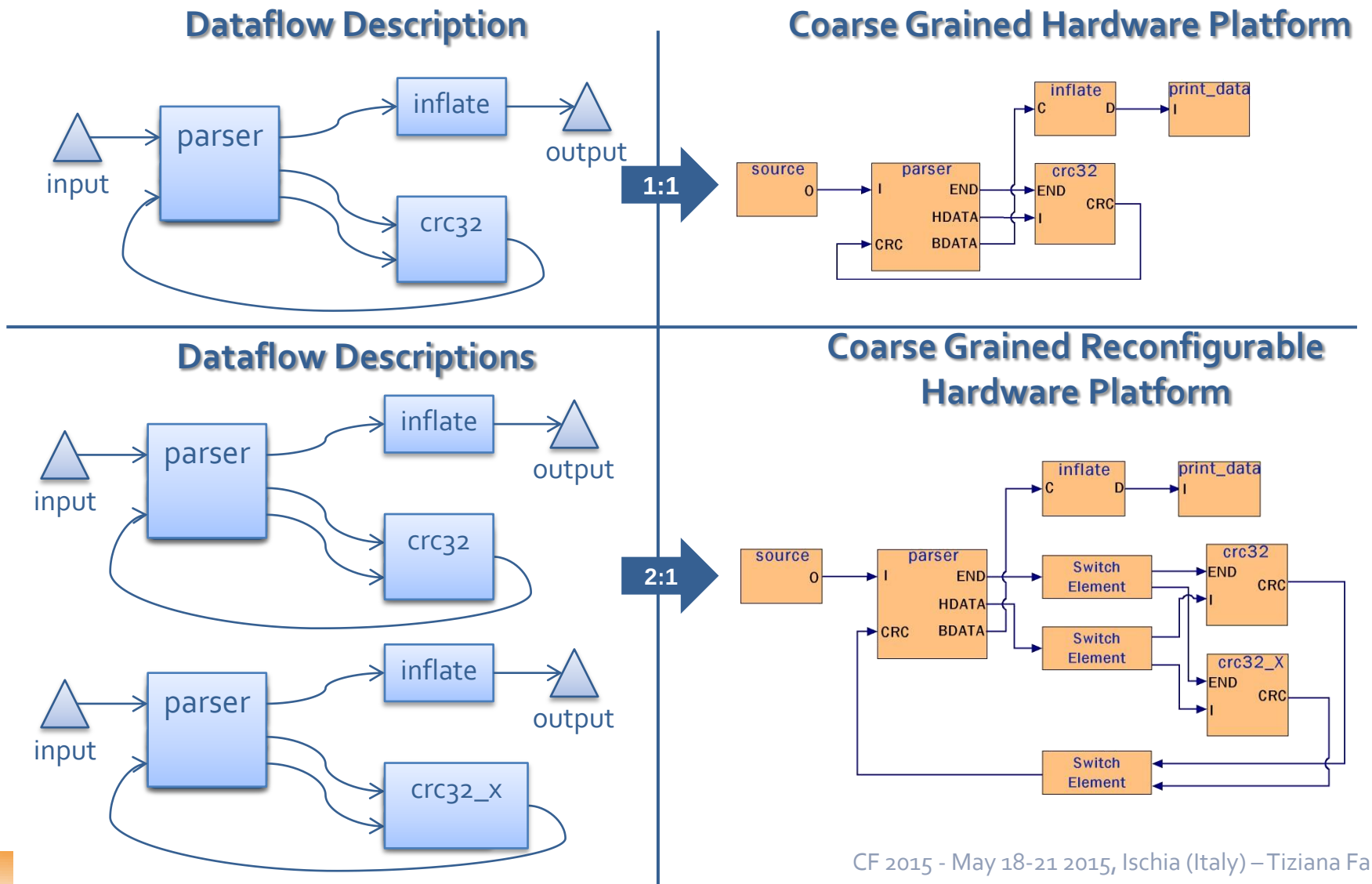

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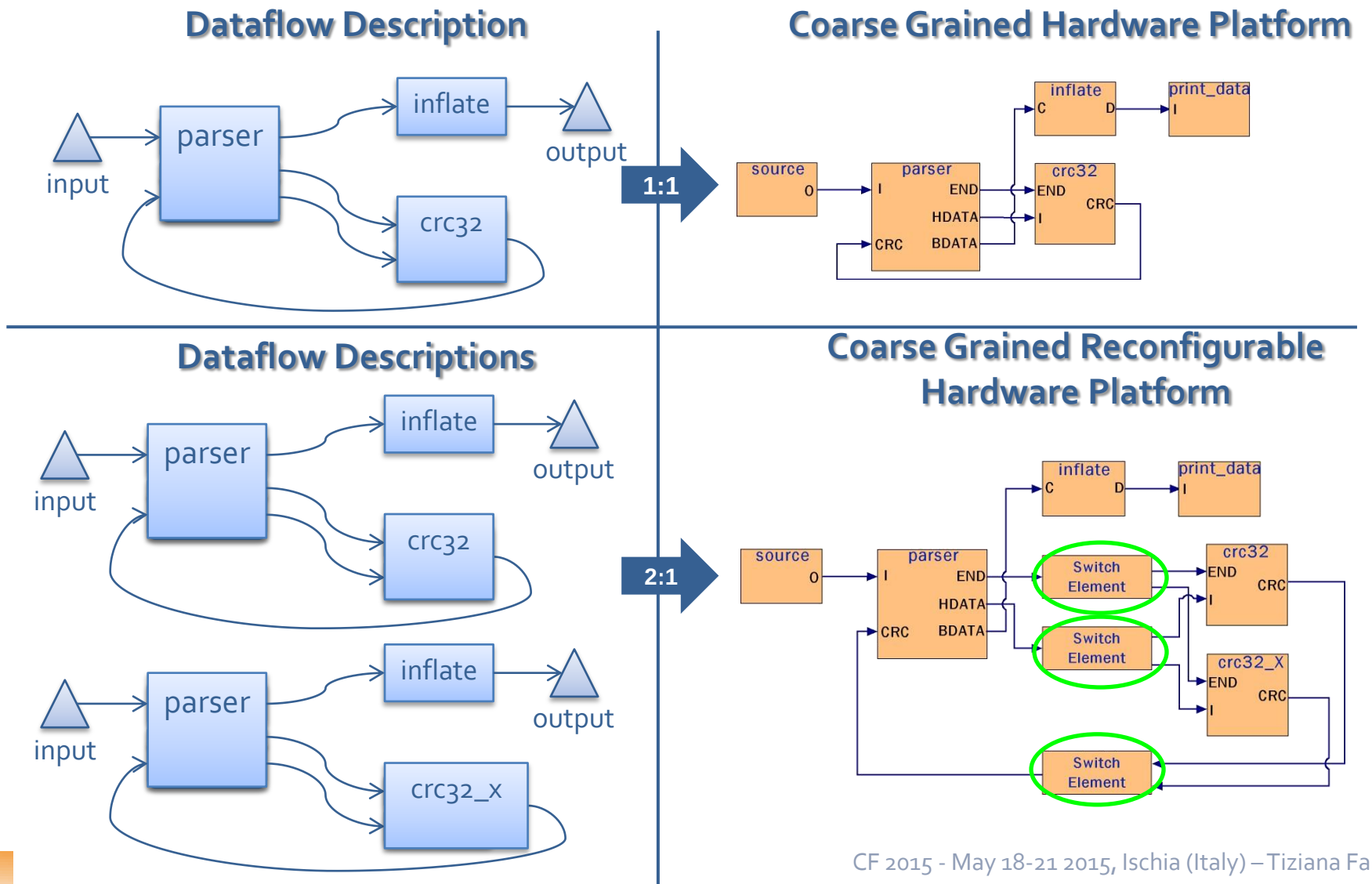

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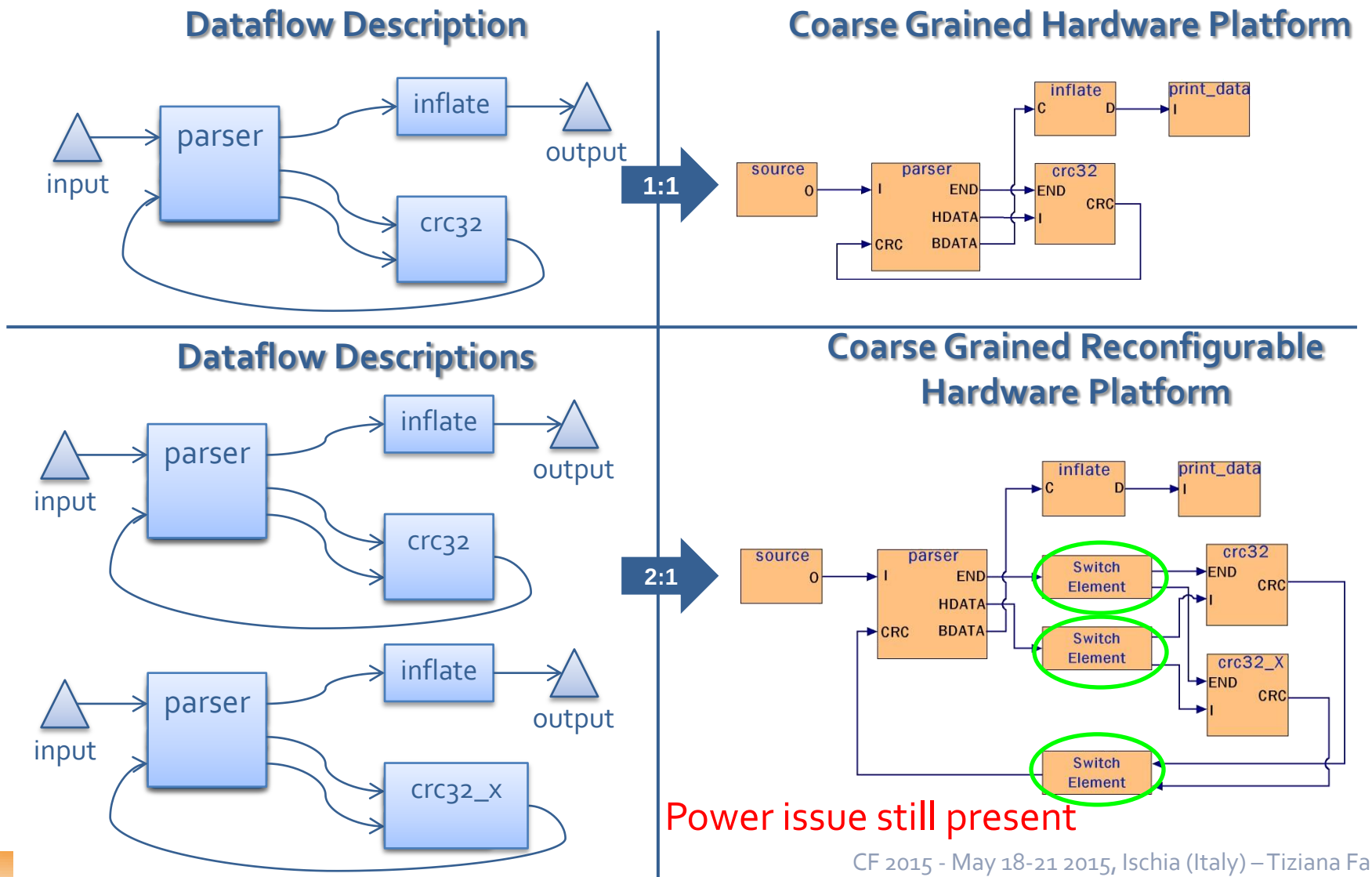

Power issue still present

Background

Power Management: Power Issue

Power consumption = Dynamic power + Static power

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- **Dynamic:**
  - **Short-circuit**: when the output line of a transistor is switching, there is a period of time when both the PMOS and the NMOS transistors are on ($I \cdot V \cdot f$)
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  - Do not depend on switching and operating frequency.
  - As transistors get smaller, their channel lengths become shorter and leakage currents increase.

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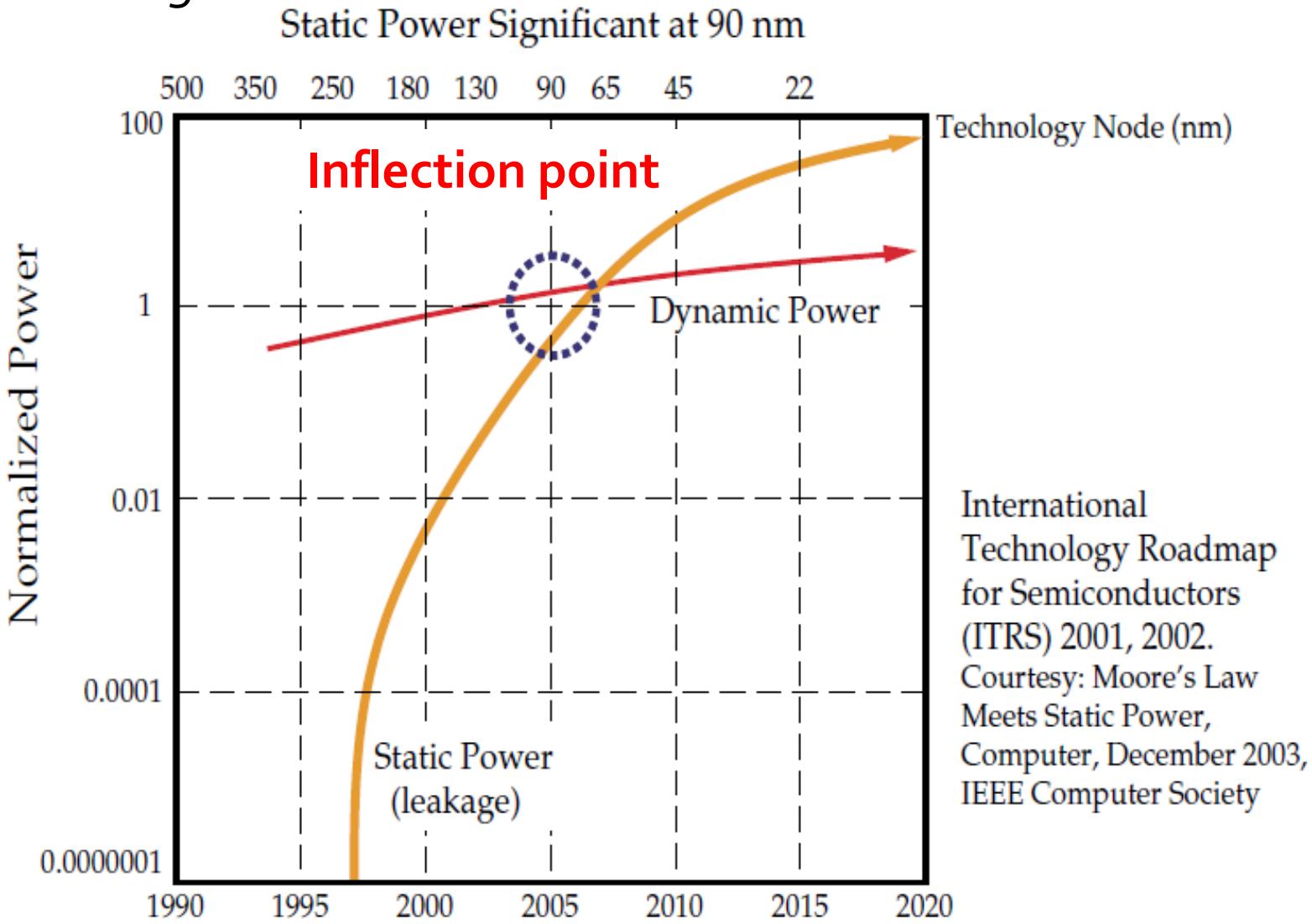
Power Management: Power Issue



International Technology Roadmap for Semiconductors (ITRS) 2001, 2002.
Courtesy: Moore's Law Meets Static Power, Computer, December 2003, IEEE Computer Society

Background

Power Management: Main Power Saving Methodologies

Dynamic Power

Clock gating
Variable frequency
Voltage islands
Multi power supply
DVFs

Leakage Power

Multi-threshold dev.
Power gating
Back (substrate) bias
Multi-oxide devices
SOI CMOS

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cadence™

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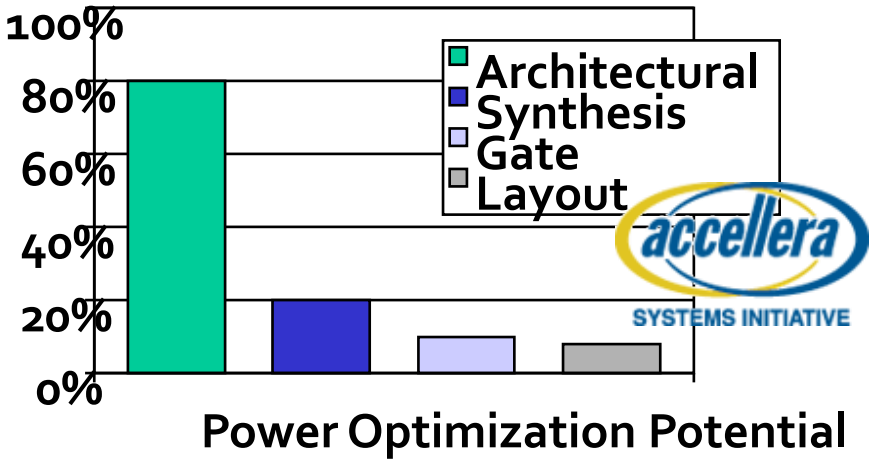

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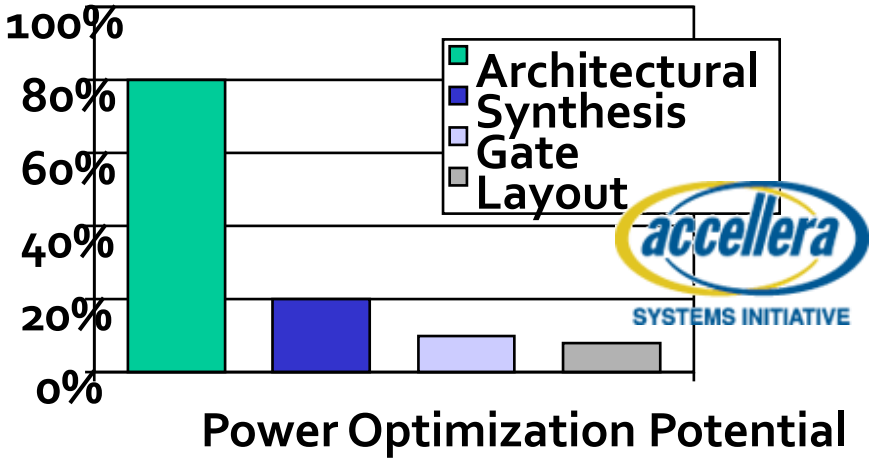

Xronos HLS Tool

coarse-grained clock gating

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

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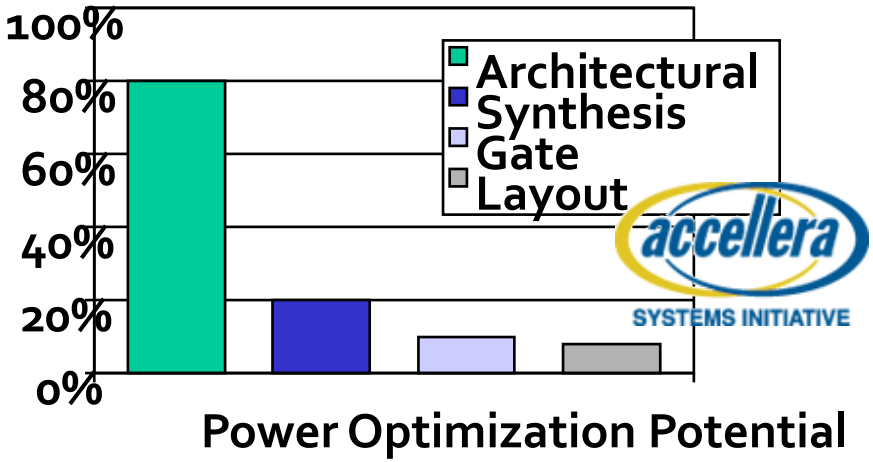

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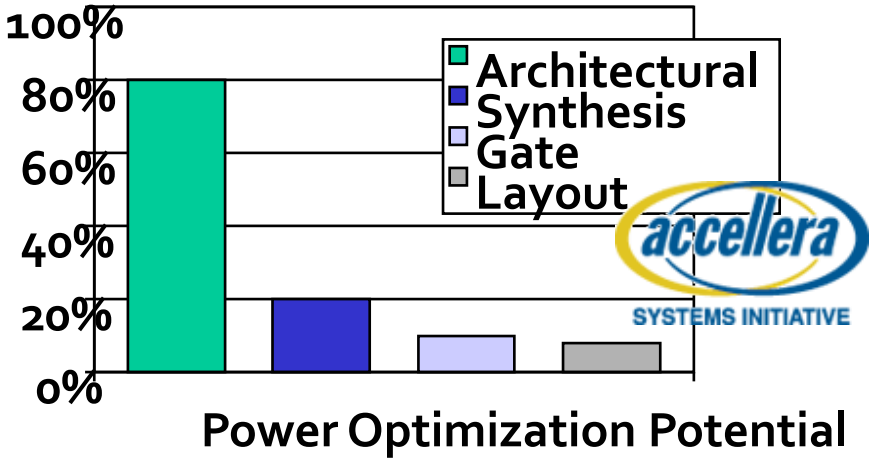

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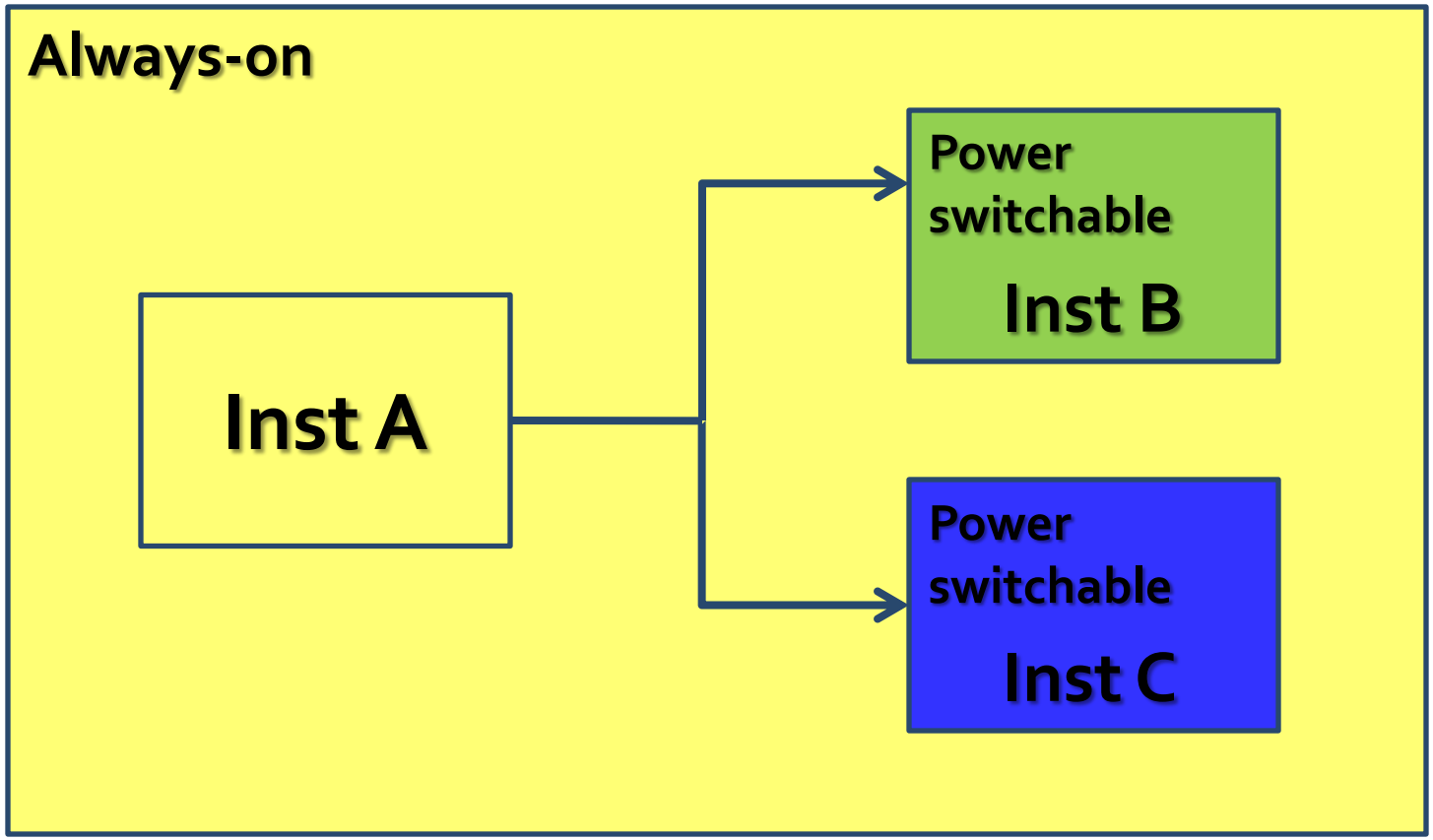
Switch off the **power supply** of design portions not involved in current computation.



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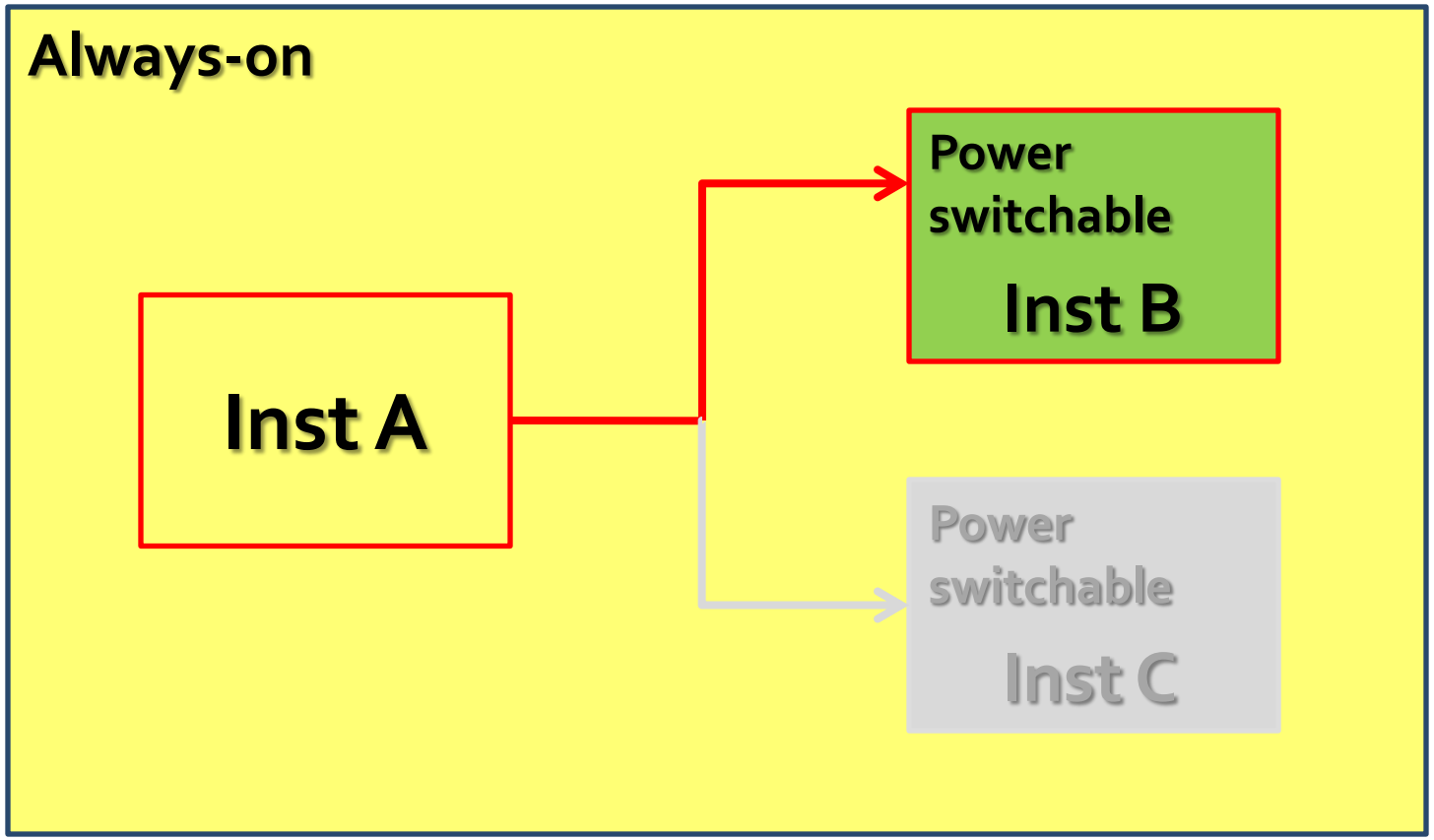

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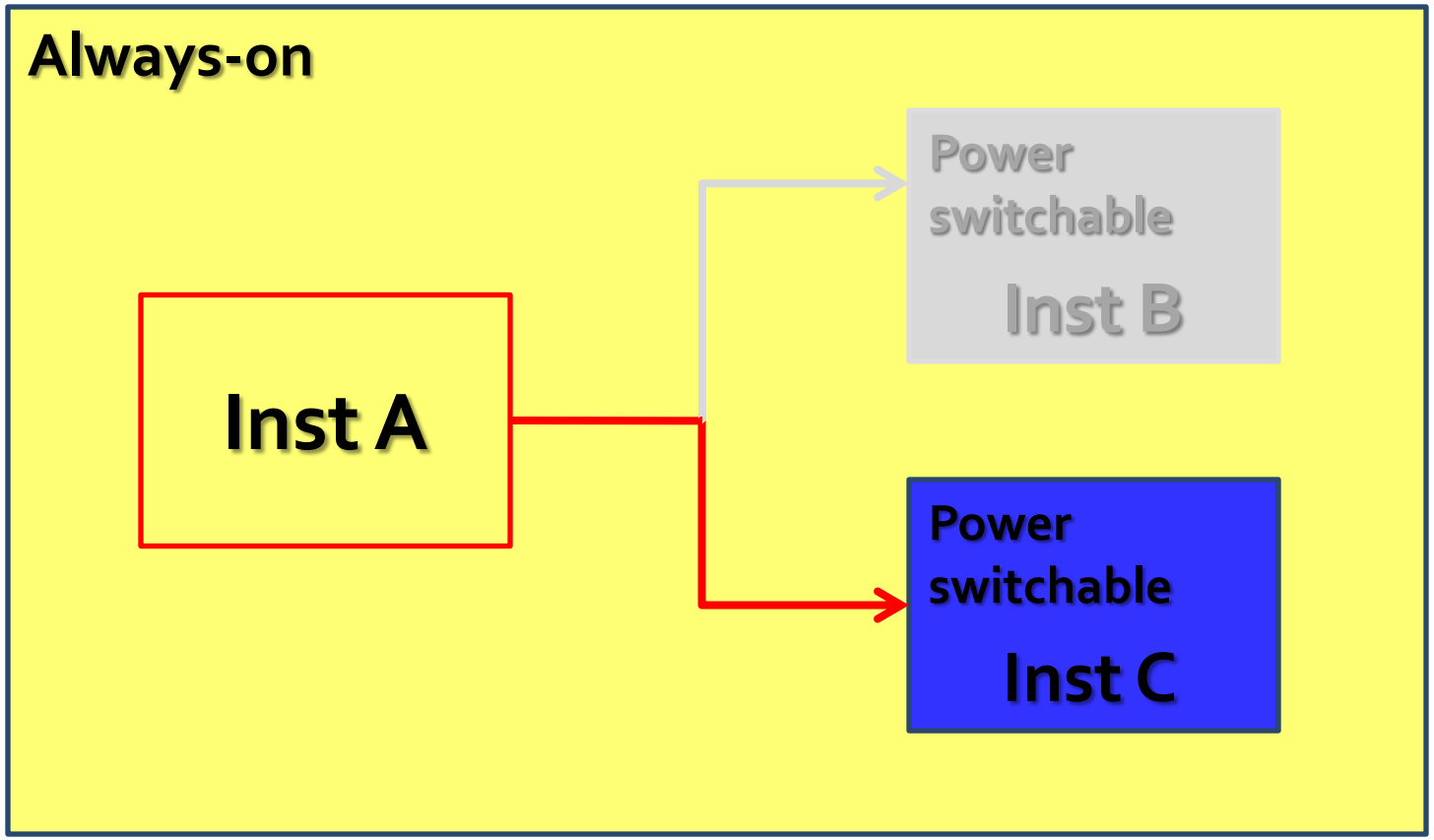

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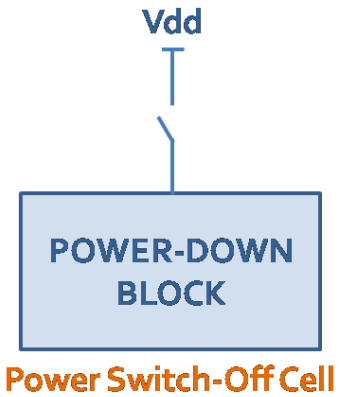

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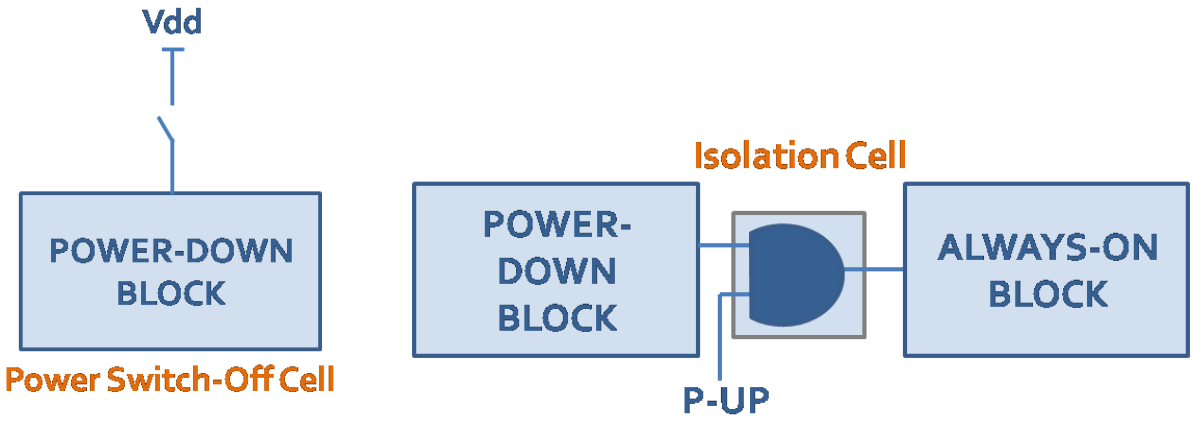

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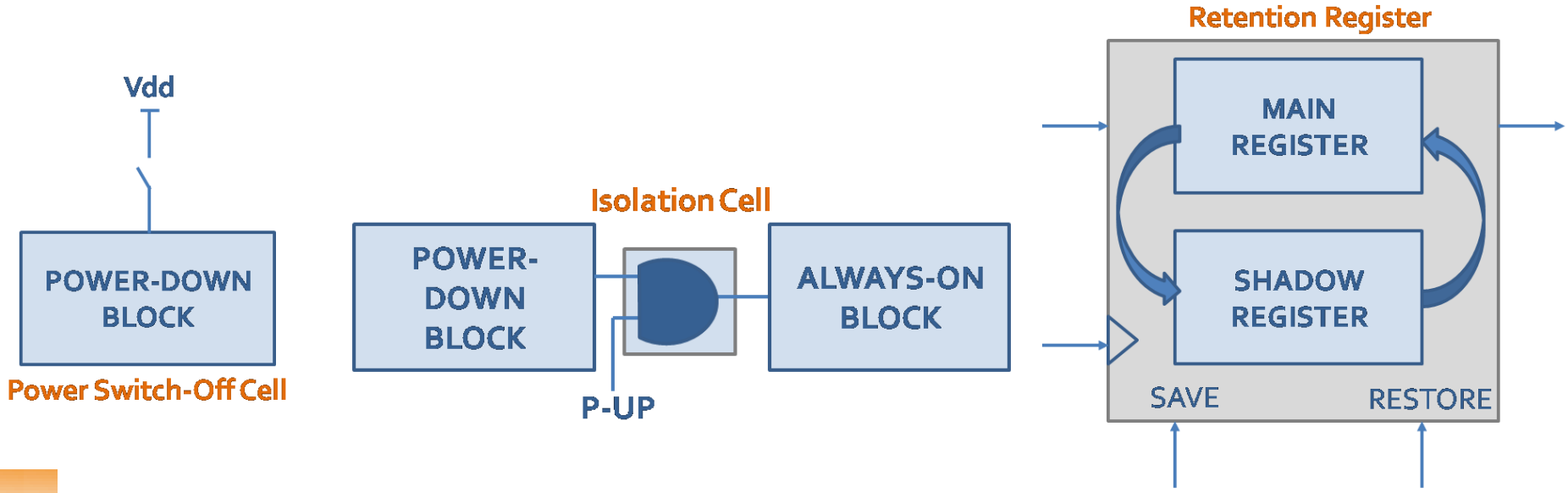

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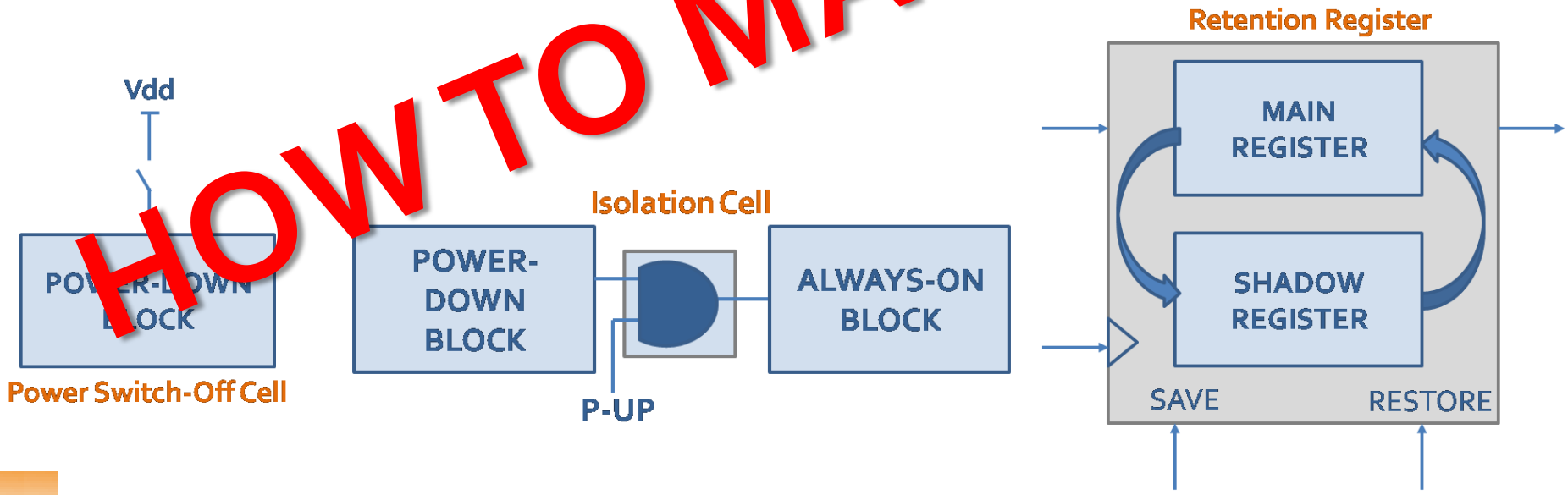
HOW TO MANAGE IT?



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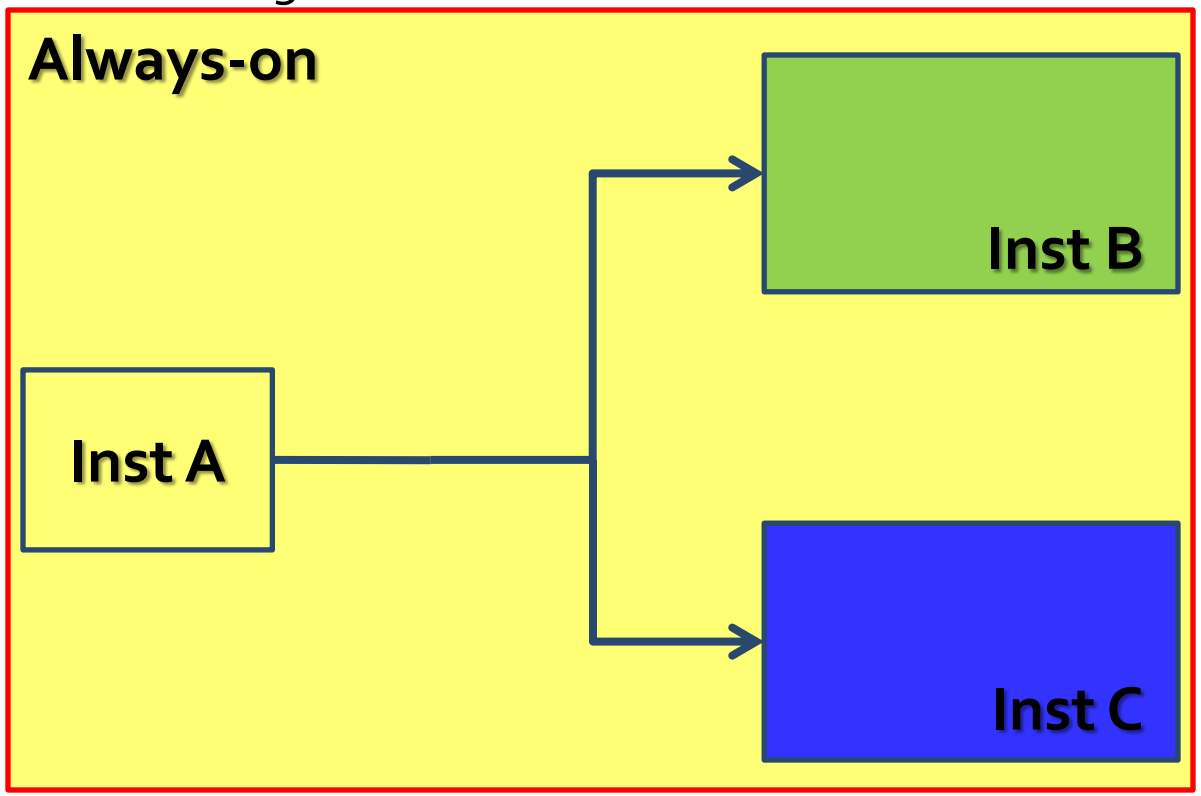
Power Management: Common Power Format

Silicon Integration Initiative



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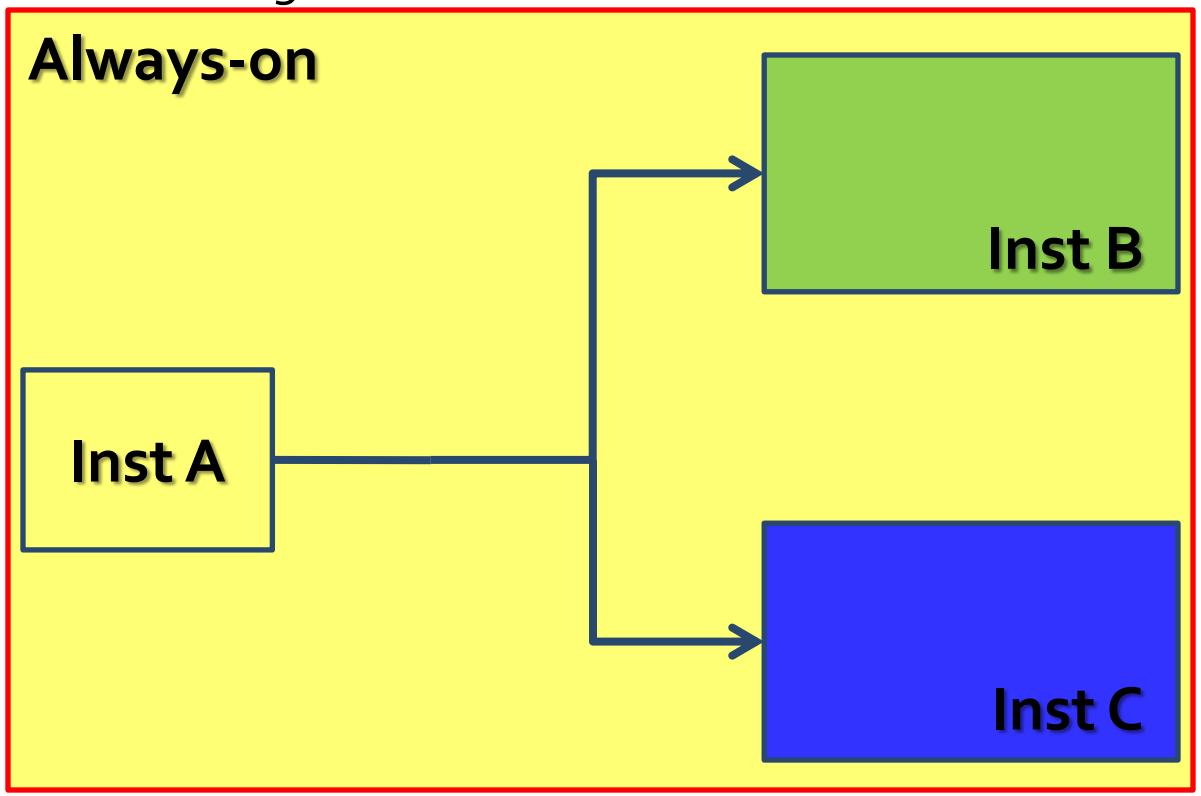

Technology part

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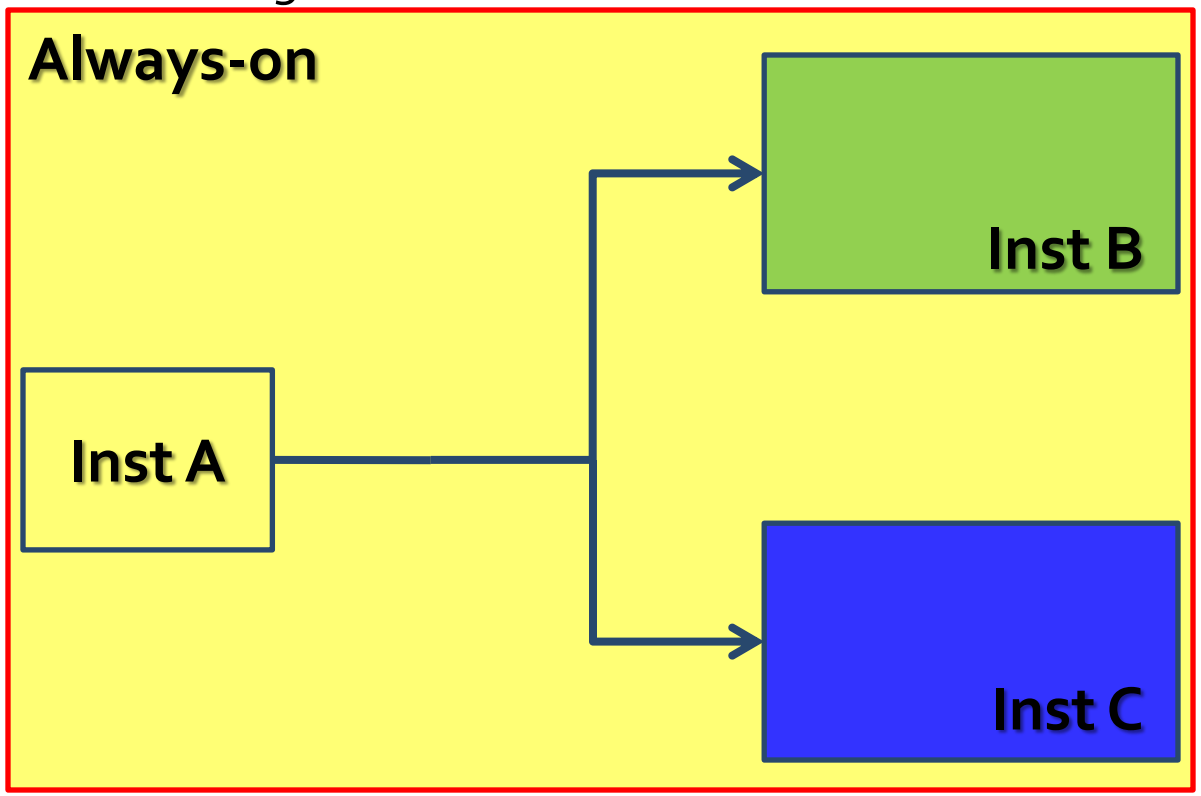

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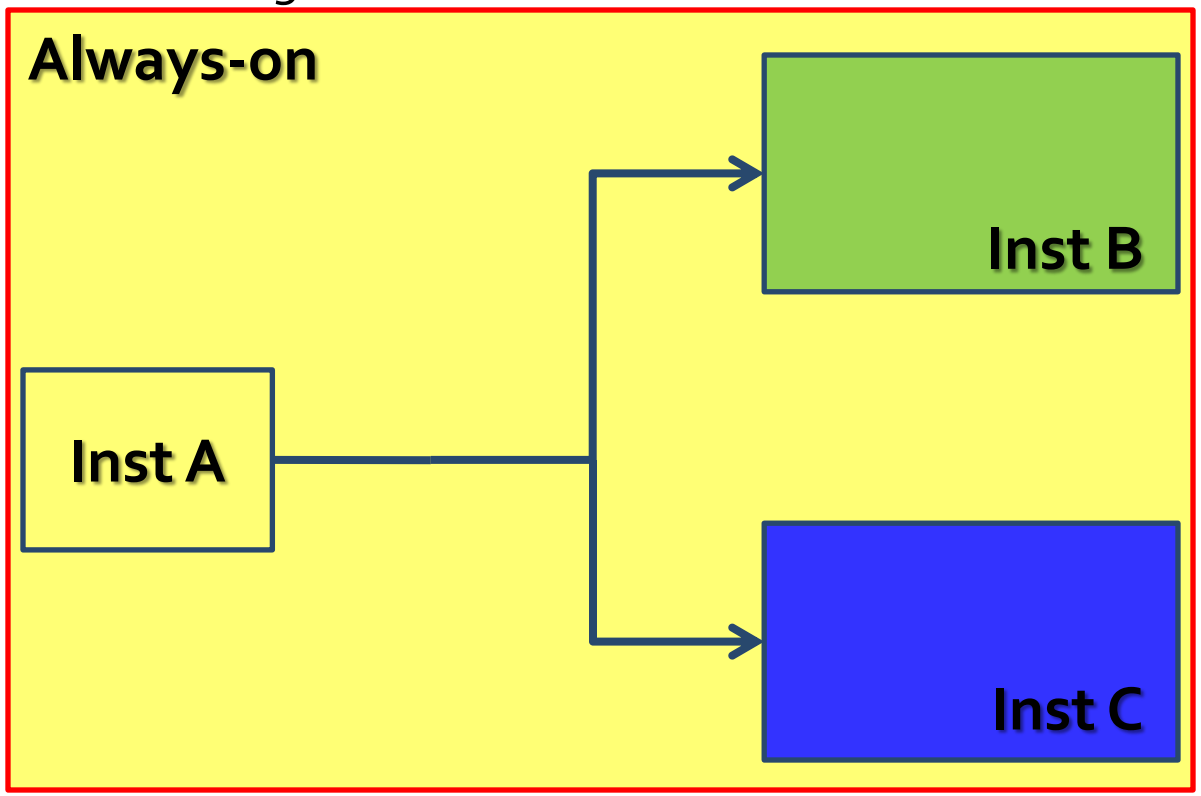

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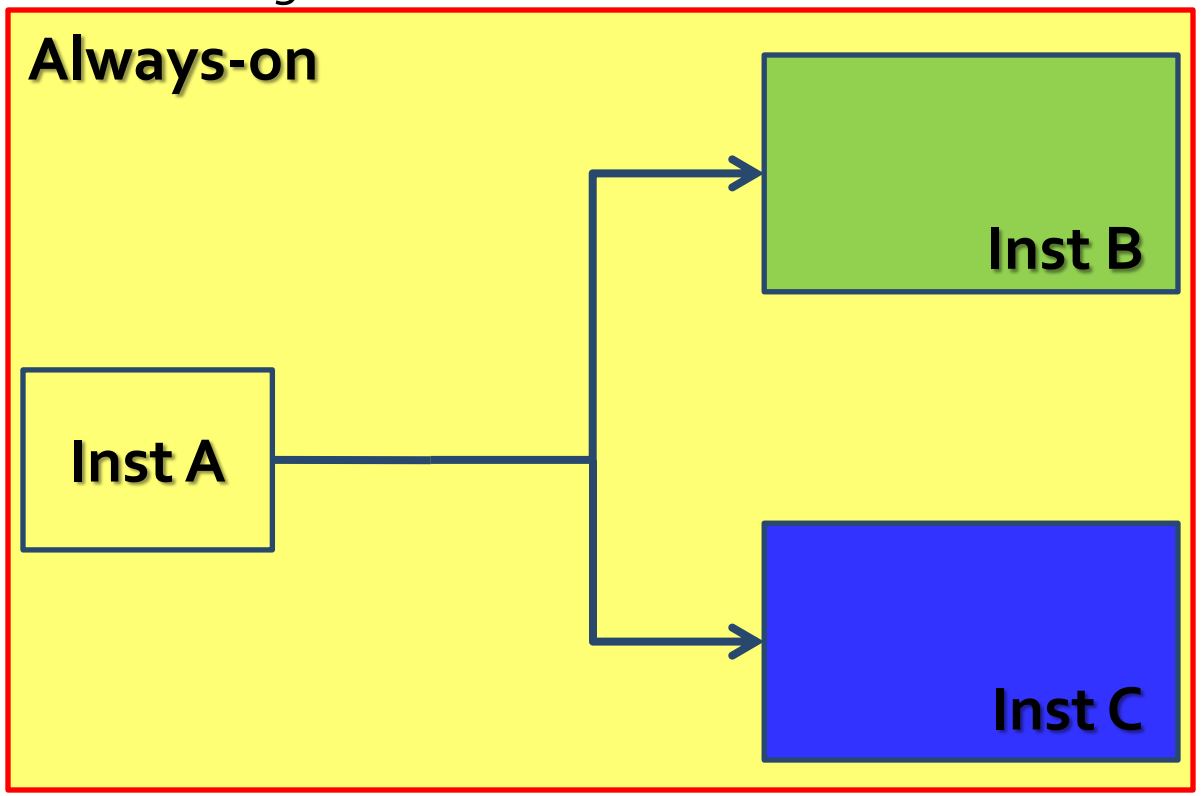

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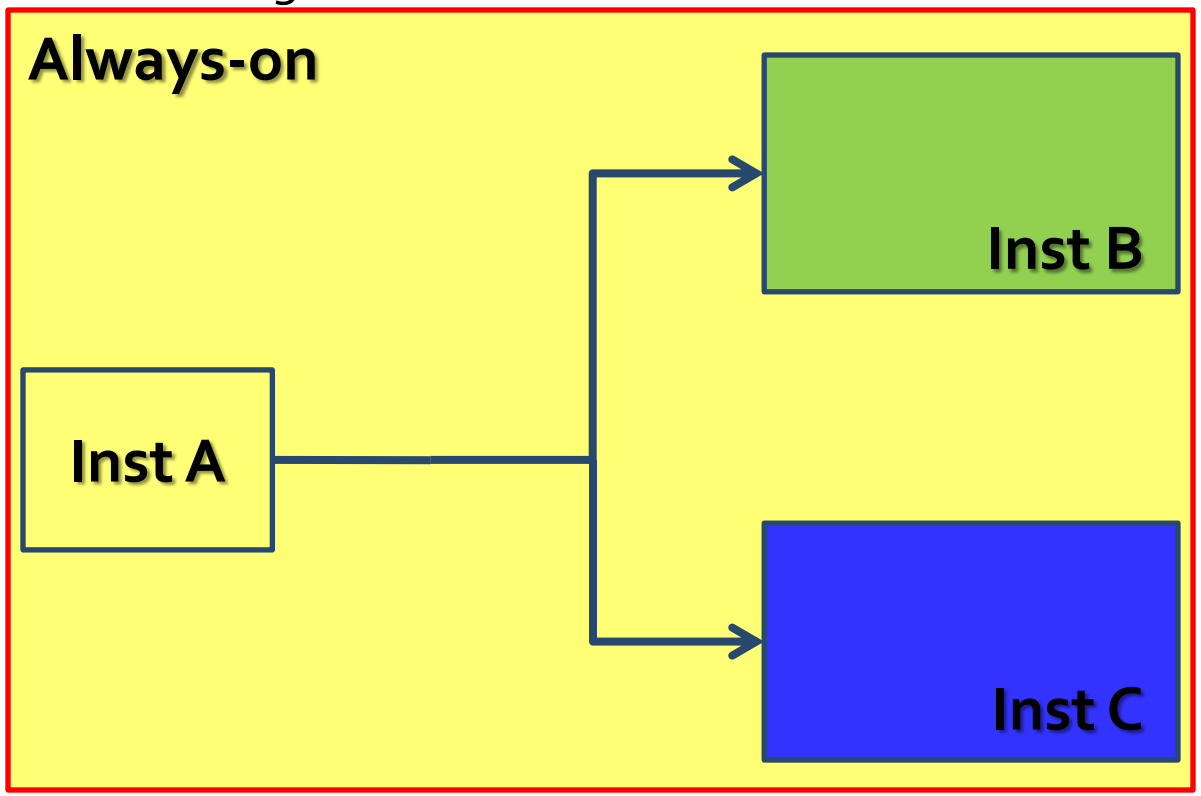

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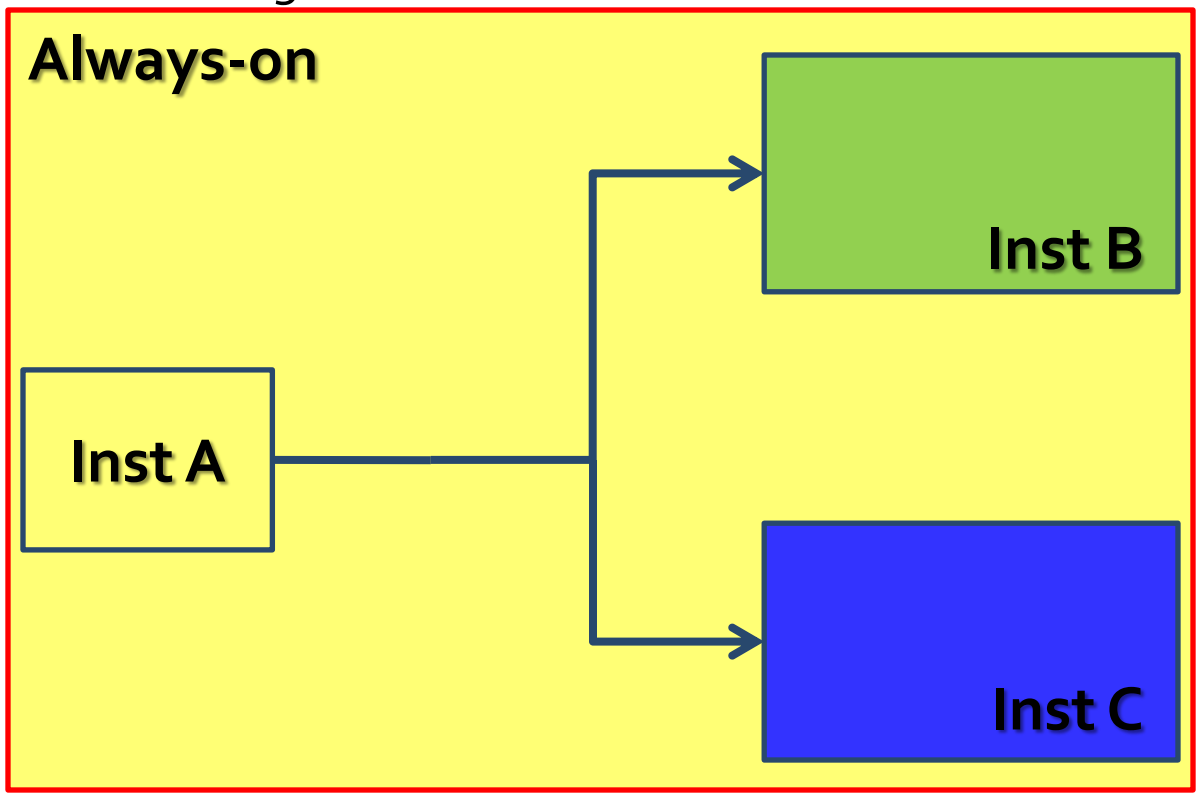

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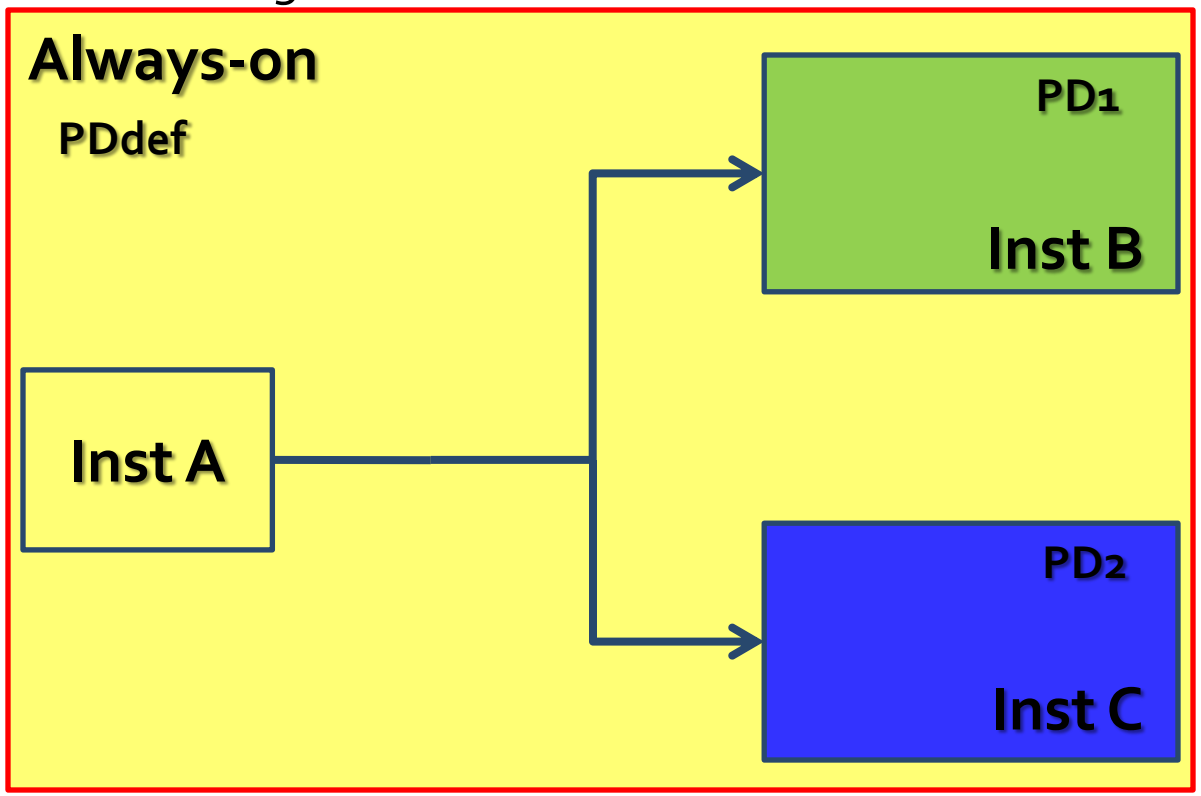

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```
create_power_domain -name PDdef –default
create_power_domain -name PD1 -instances {inst_A } \

create_power_domain -name PD2 -instances {inst_AB} \
```

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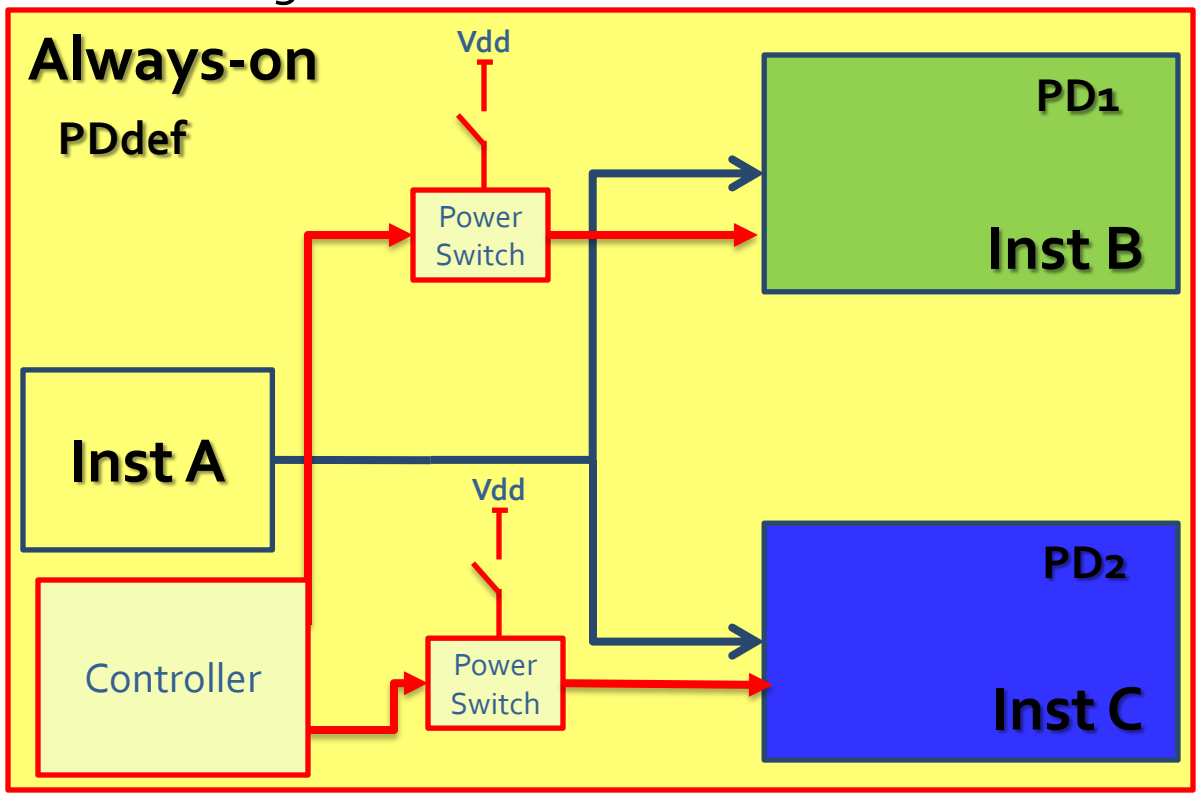

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```
create_power_domain -name PDdef –default
create_power_domain -name PD1 -instances {inst_A } \
-shutoff_condition {contr/pso1}
create_power_domain -name PD2 -instances {inst_AB} \
-shutoff_condition {contr/pso2}
```

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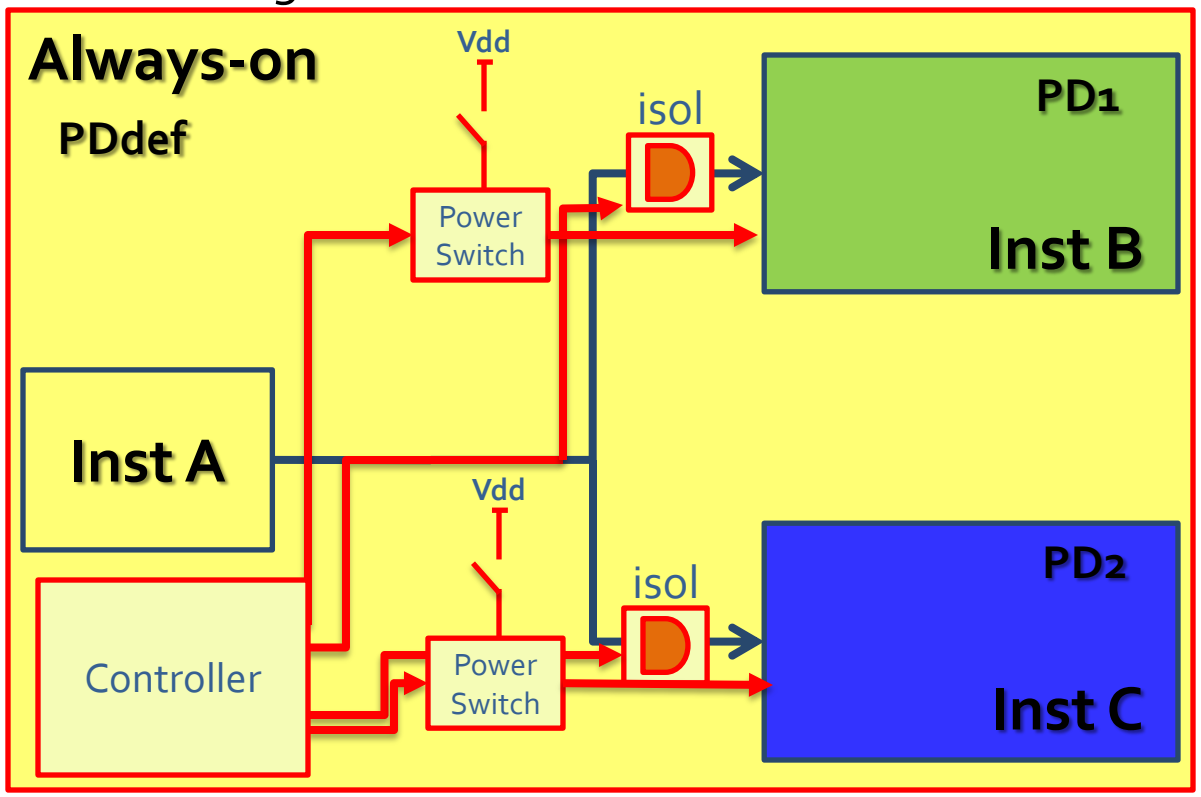

create_isolation_rule -name iso1 –to PD1 \
-isolation_condition {contr/iso1}
create_isolation_rule -name iso2 –to PD2 \
-isolation_condition {contr/iso2}

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#individuate low power cells
define_xxx cell

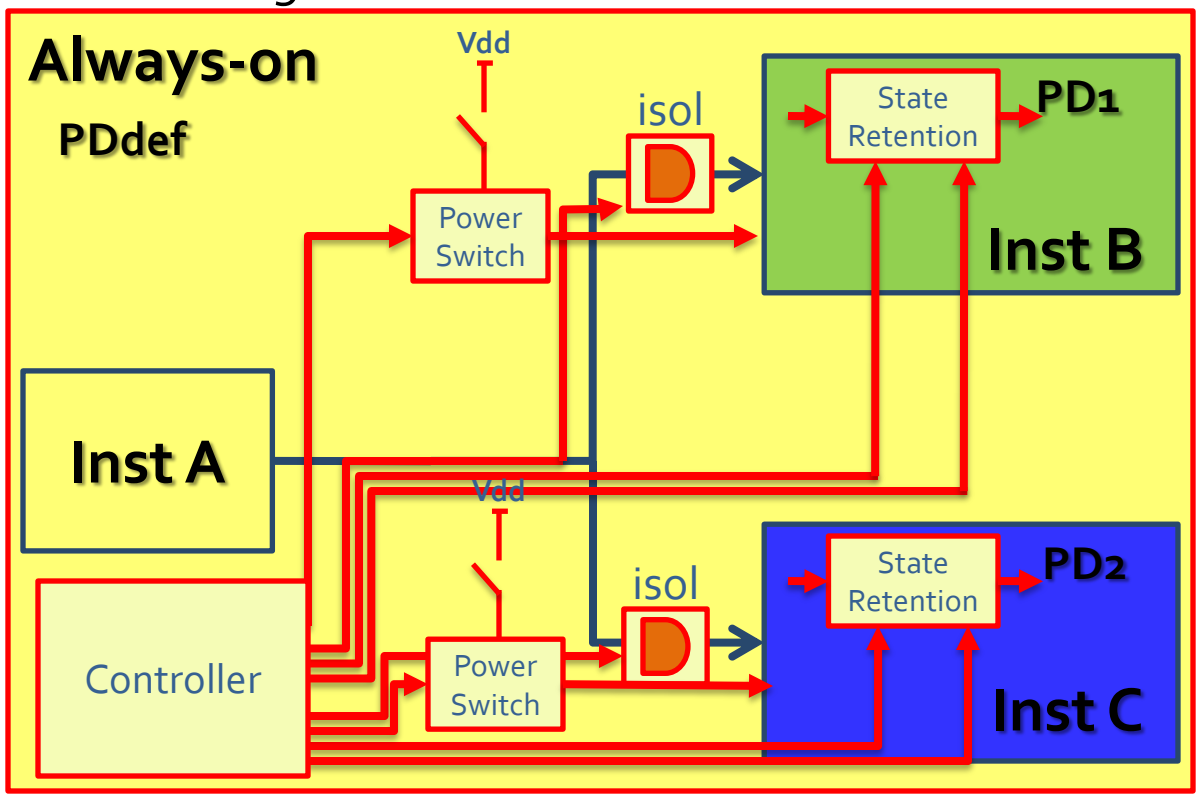
Power Intent part
#instantiate low power cells
create_xxx_rule

#more details for
#implementation tools
update_xxx_rule

Background

Power Management: Common Power Format

Silicon Integration Initiative



Technology part

#individuate low power cells

define_xxx cell

Power Intent part

#instantiate low power cells

create_xxx_rule

#more details for

#implementation tools

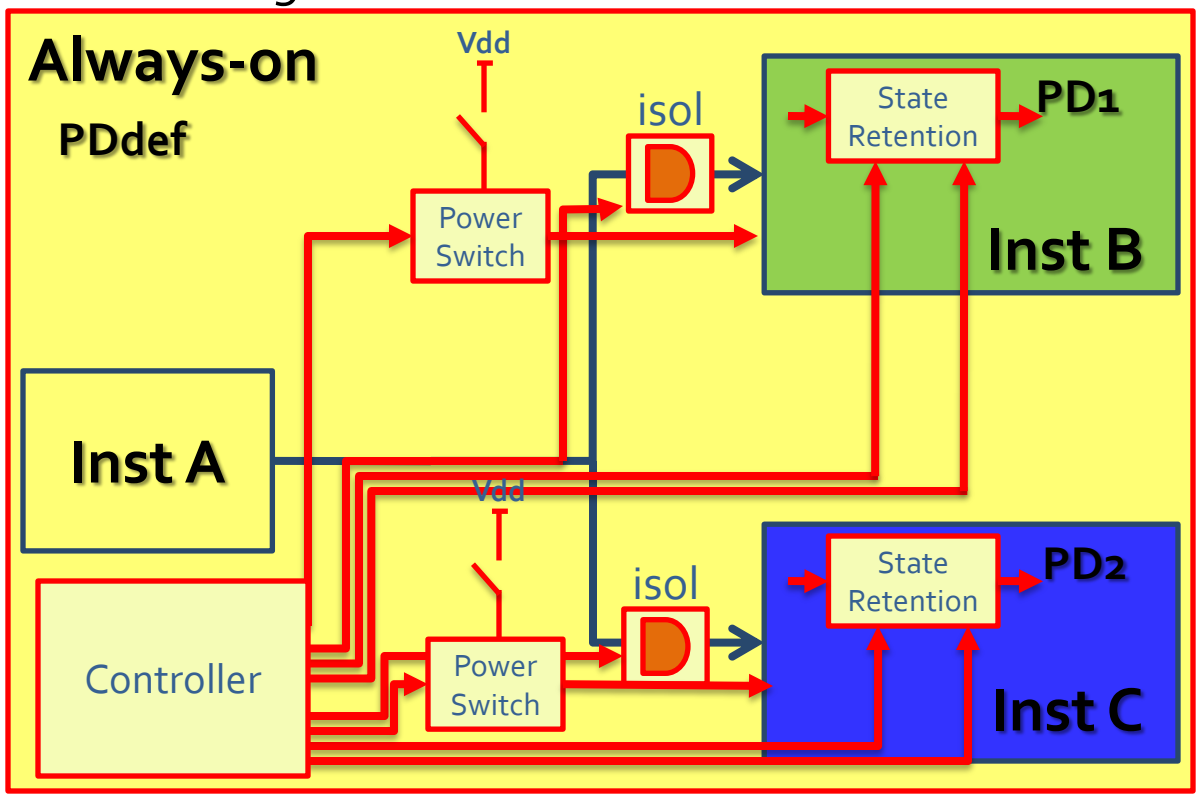
update_xxx_rule

```
create_state_retention_rule -name st1 -domain PD1\
-restore_edge {contr/rstr1} -save_edge {contr/save1}
create_state_retention_rule -name st2 -domain PD2\
-restore_edge {contr/rstr2} -save_edge {contr/save2}
```

Background

Power Management: Common Power Format

Silicon Integration Initiative




```
create_state_retention_rule -name st1 -domain PD1\
-restore_edge {contr/rstr1} -save_edge {contr/save1}
create_state_retention_rule -name st2 -domain PD2\
-restore_edge {contr/rstr2} -save_edge {contr/save2}
```

Technology part

#individuate low power cells

define_xxx cell

Power Intent part

#instantiate low power cells

create_xxx_rule

#more details for

#implementation tools

update_xxx_rule

3 Power Domains	
Interfaces	**Signals**
3 create_domain	2 switch-off signals
2 create isolation	2 isolation signals
2 create retention	2 save signals 2 restore signals
TOT: 7 interfaces	**TOT: 8 signals**

Background

Power Management: Common Power Format

Silicon Integration Initiative

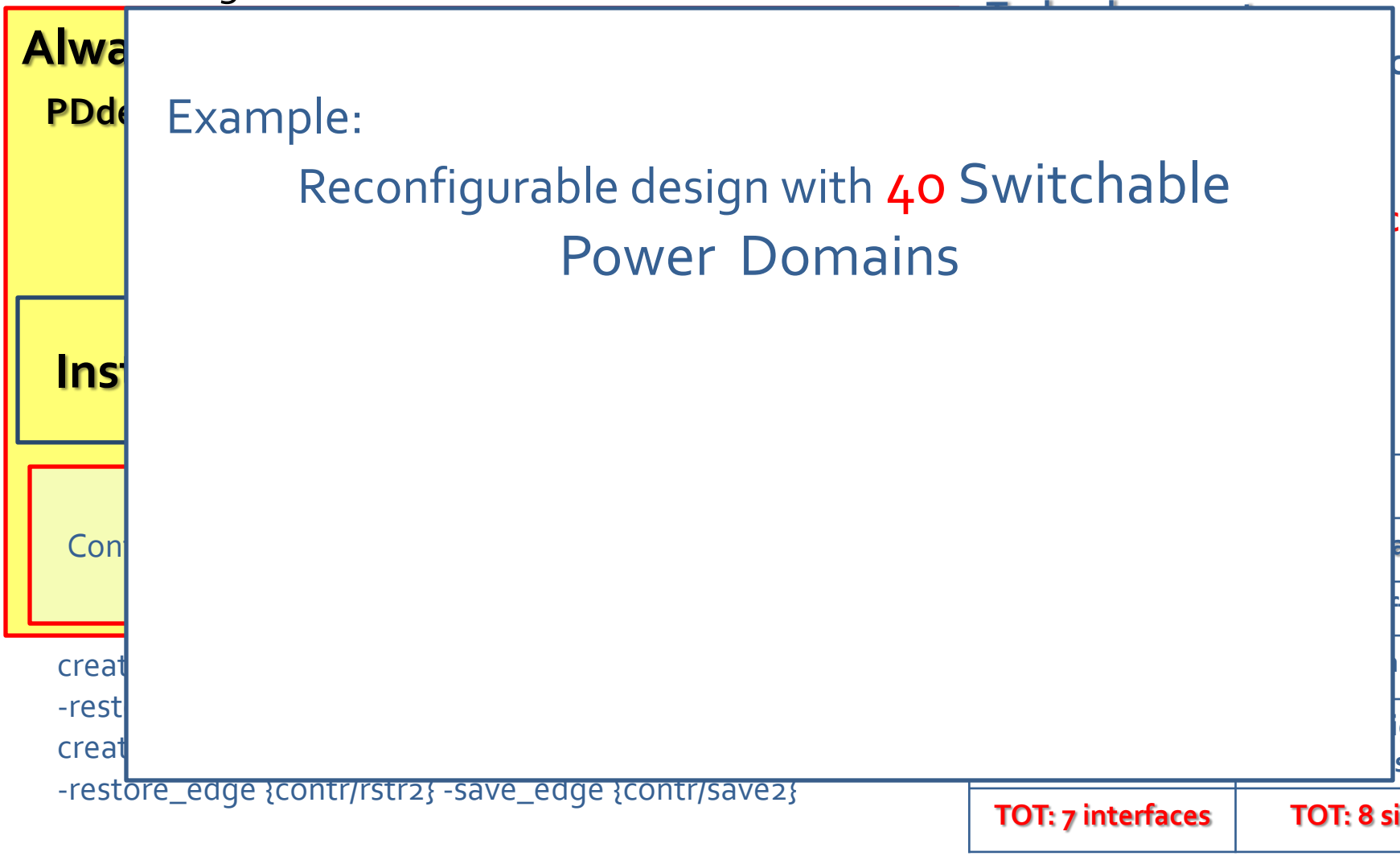
Background

Power Management: Common Power Format

Silicon Integration Initiative

Example:

Reconfigurable design with 40 Switchable Power Domains



Background

Power Management: Common Power Format

Silicon Integration Initiative

Example:

Reconfigurable design with 40 Switchable Power Domains

Need to define switch-off domains, isolation and state retention

3 * 40 = 120 interfaces

Background

Power Management: Common Power Format

Silicon Integration Initiative

Example:

Reconfigurable design with 40 Switchable Power Domains

Need to define switch-off domains, isolation and state retention

3 * 40 = 120 interfaces

Create enable signals

(1*switch-off + 1 * isol + 2*rtn)*40 = 160 signals

	als
	ff signals
	signals
	gnals signals
TOT: 7 interfaces	TOT: 8 signals

Background

Power Management: Common Power Format

Silicon Integration Initiative

Example:

Reconfigurable design with 40 Switchable Power Domains

NEED AUTOMATIC FLOW

Create enable signals

(1*switch-off + 1 * isol + 2*rtn)*40 = 160 signals

creat
-rest
creat
-restore_edge {contr/rstr2} -save_edge {contr/save2}

	als
	ff signals
	signals
	gnals signals
TOT: 7 interfaces	TOT: 8 signals

Outline

- Introduction
  - Increasing Complexity
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  - Dataflow Model of Computation
  - Coarse-Graine Reconfiguration: Multi-Dataflow Composer Tool - MDC
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  - Experimental Results
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Automated Power Gating

Logic Regions Identification

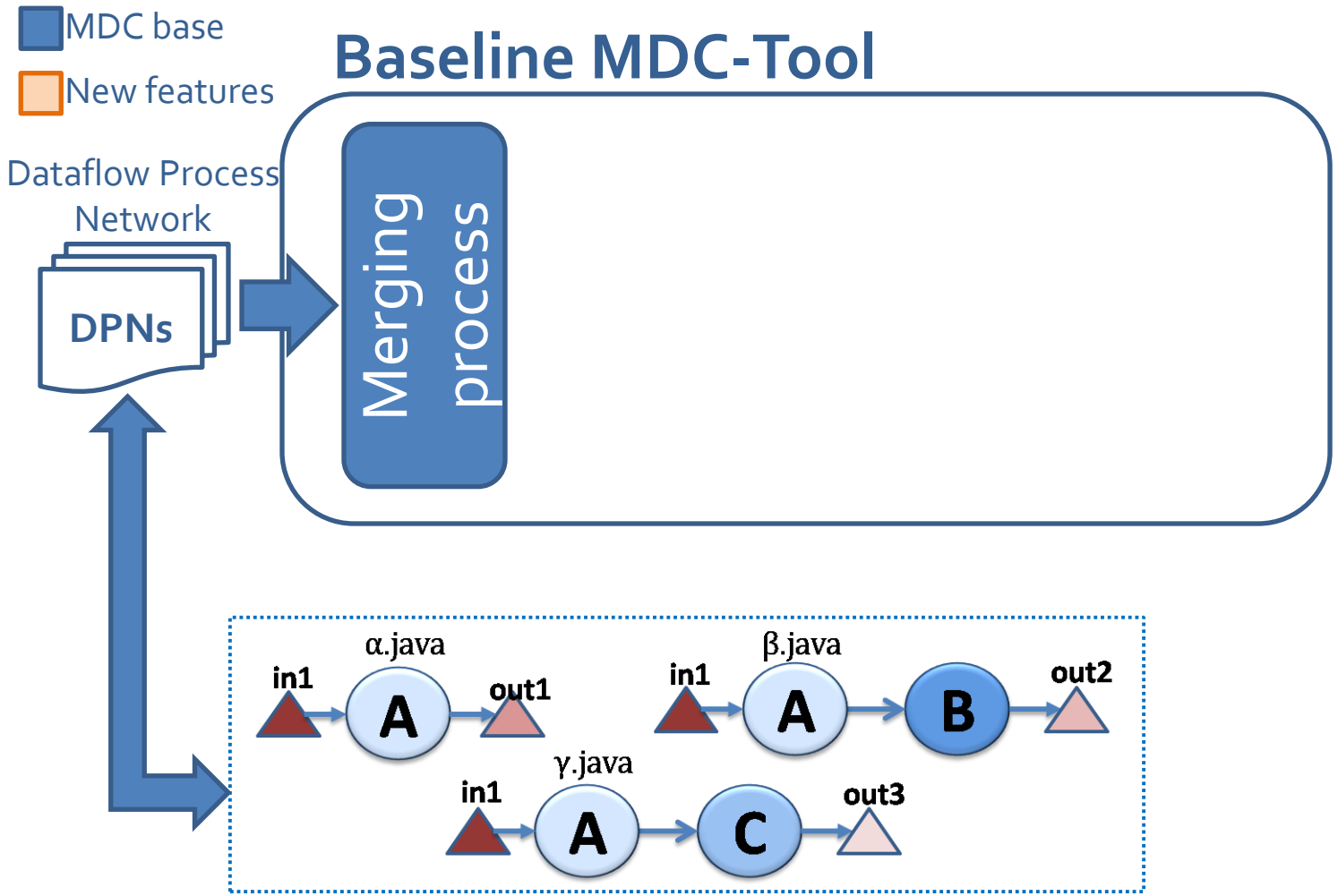
MDC base

New features

Baseline MDC-Tool

Automated Power Gating

Logic Regions Identification



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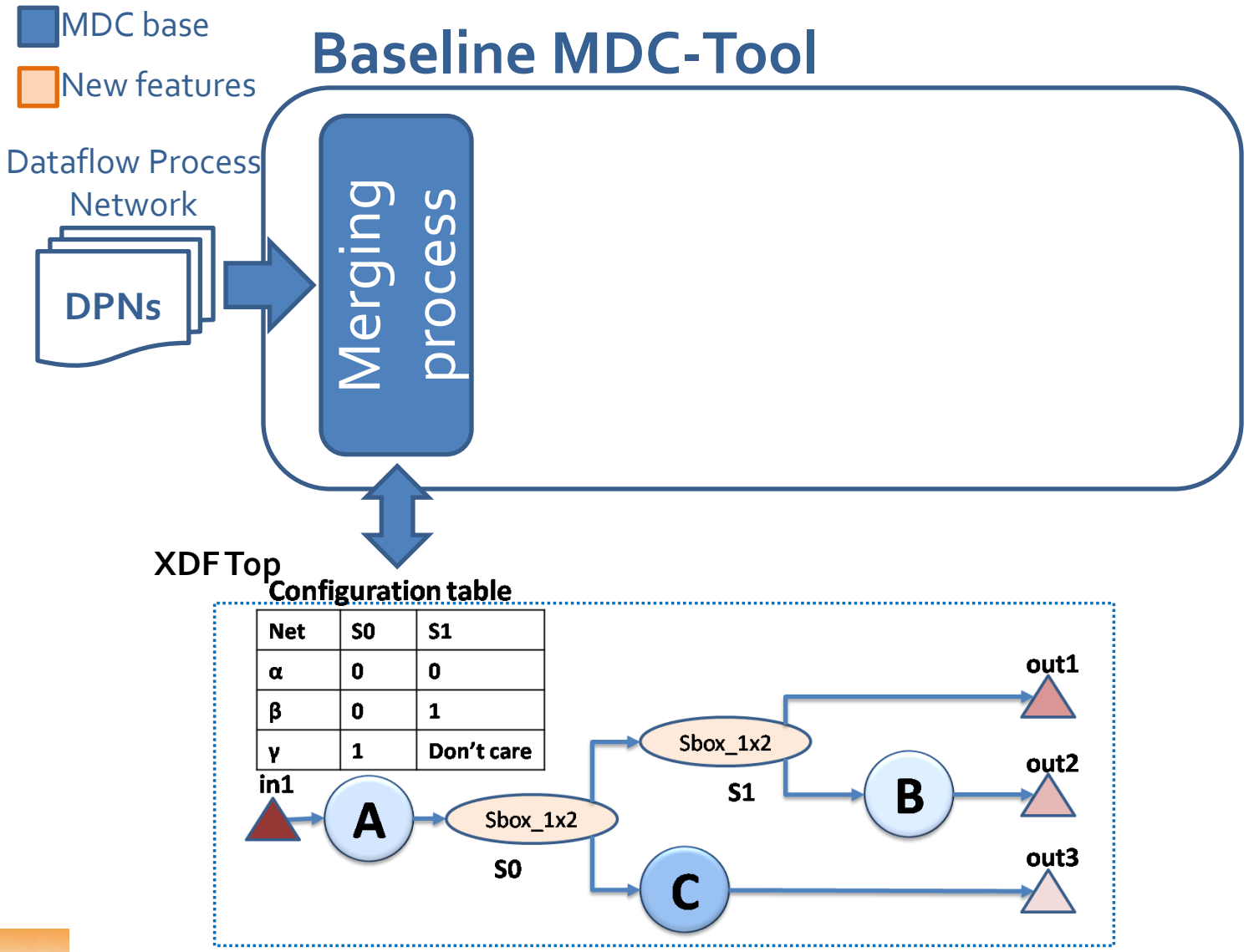
Logic Regions Identification



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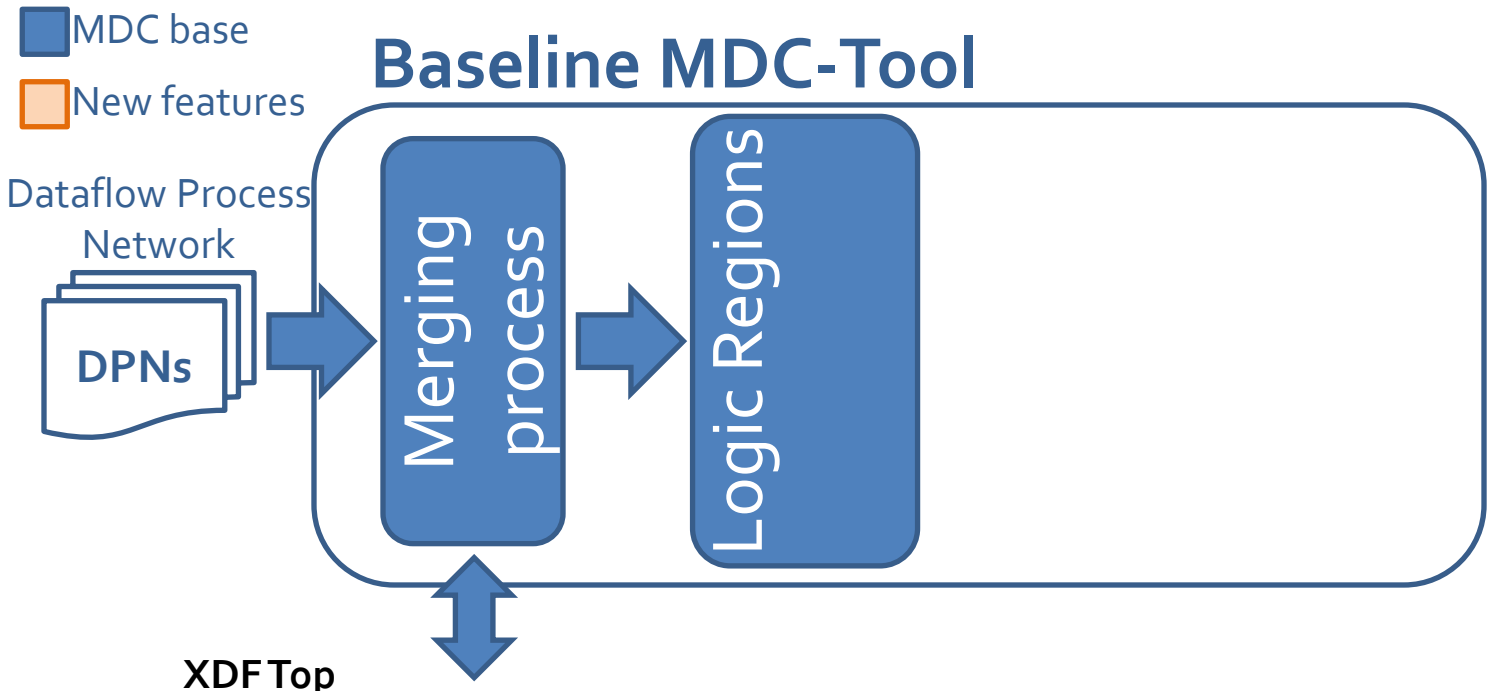
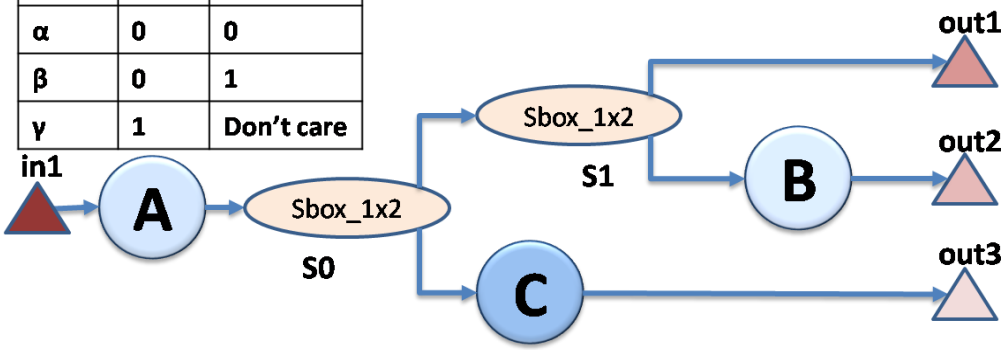


Configuration table

Net	S0	S1
α	0	0
β	0	1
γ	1	Don't care



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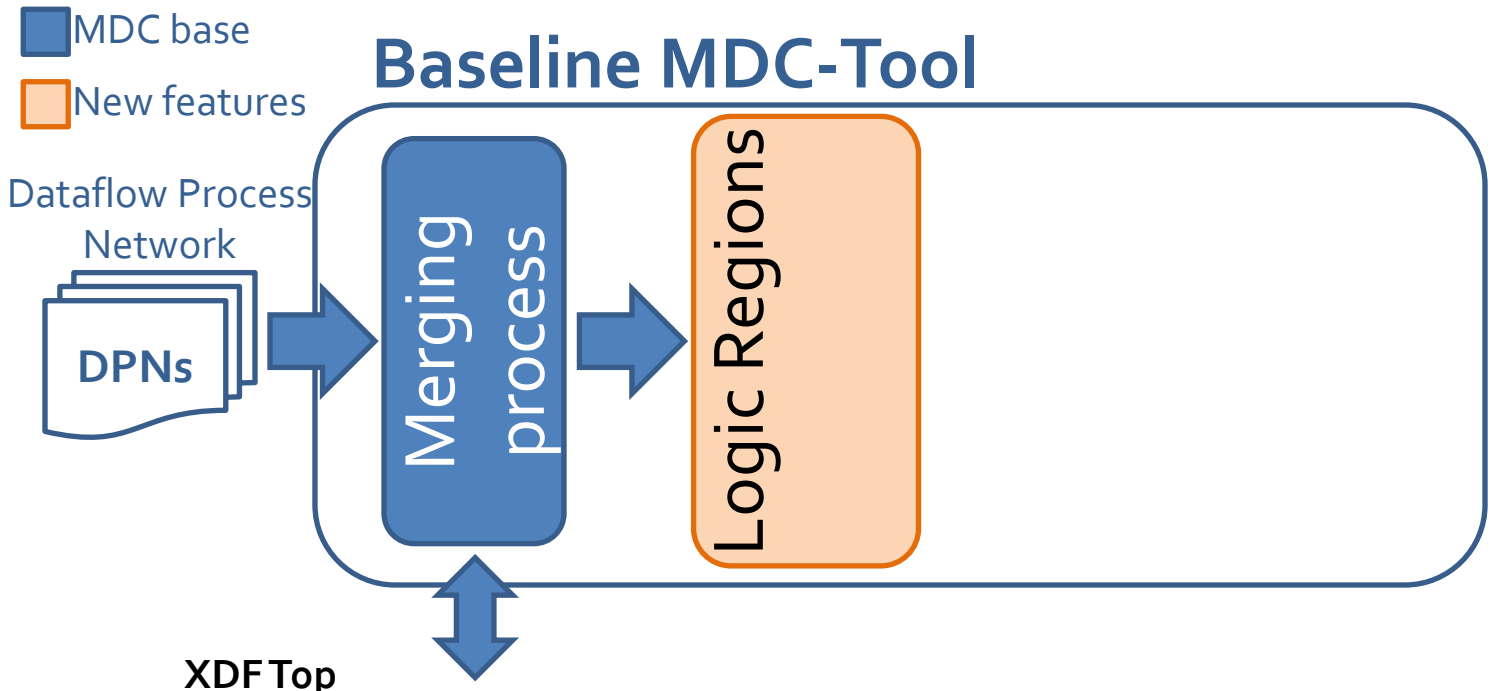

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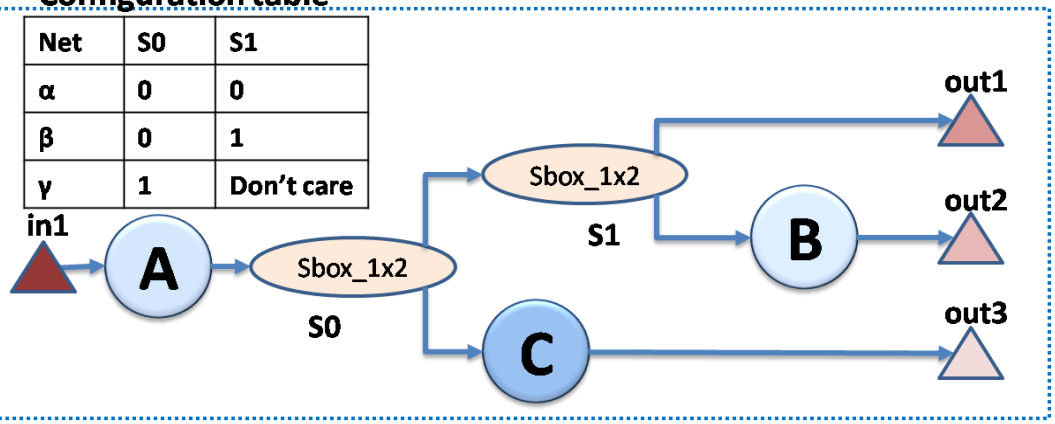

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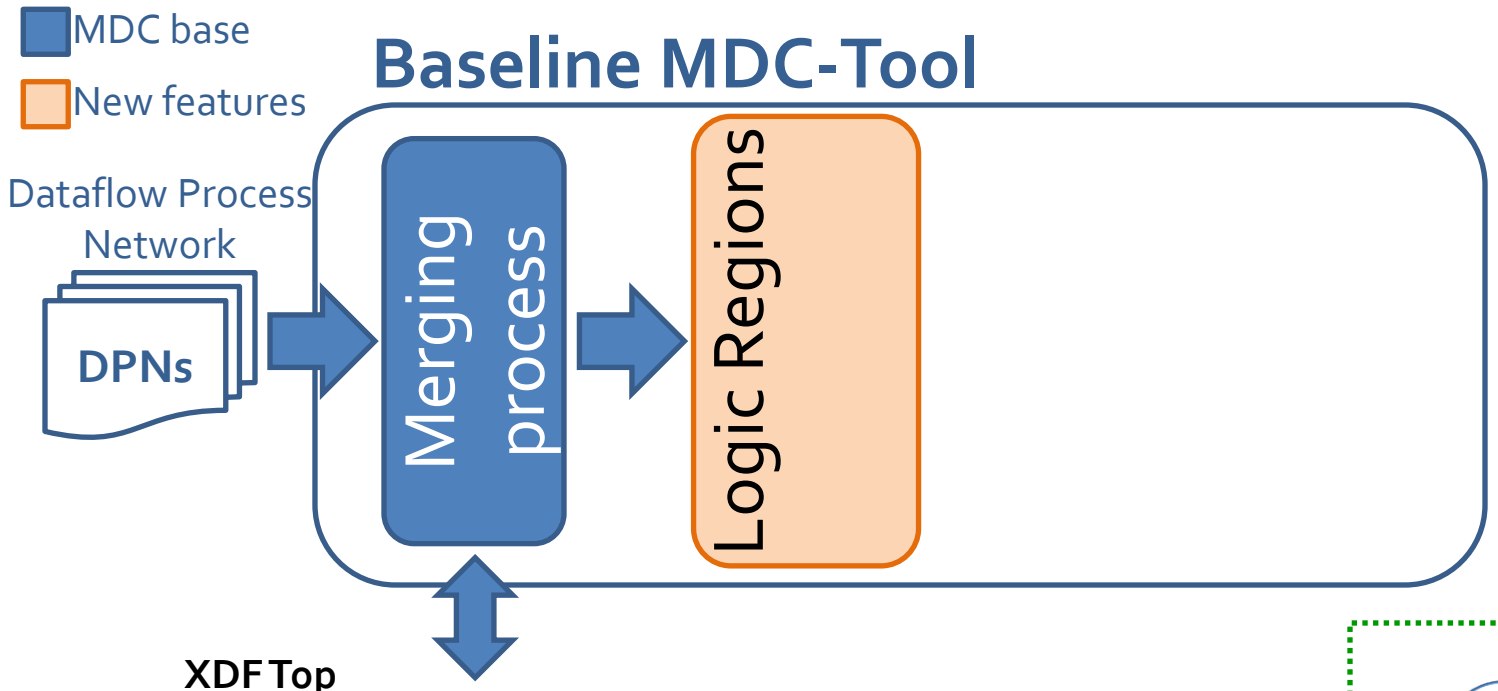

XDF Top

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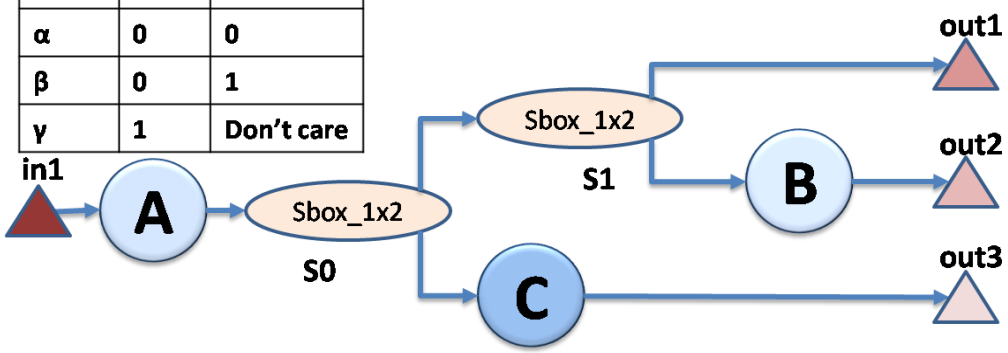
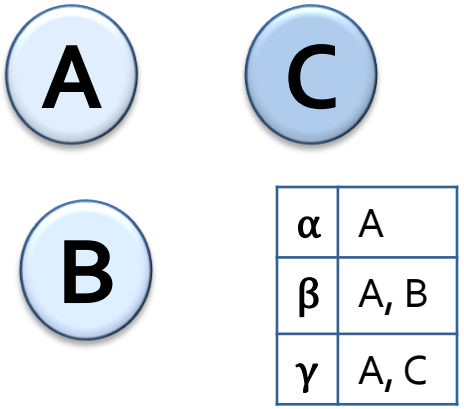
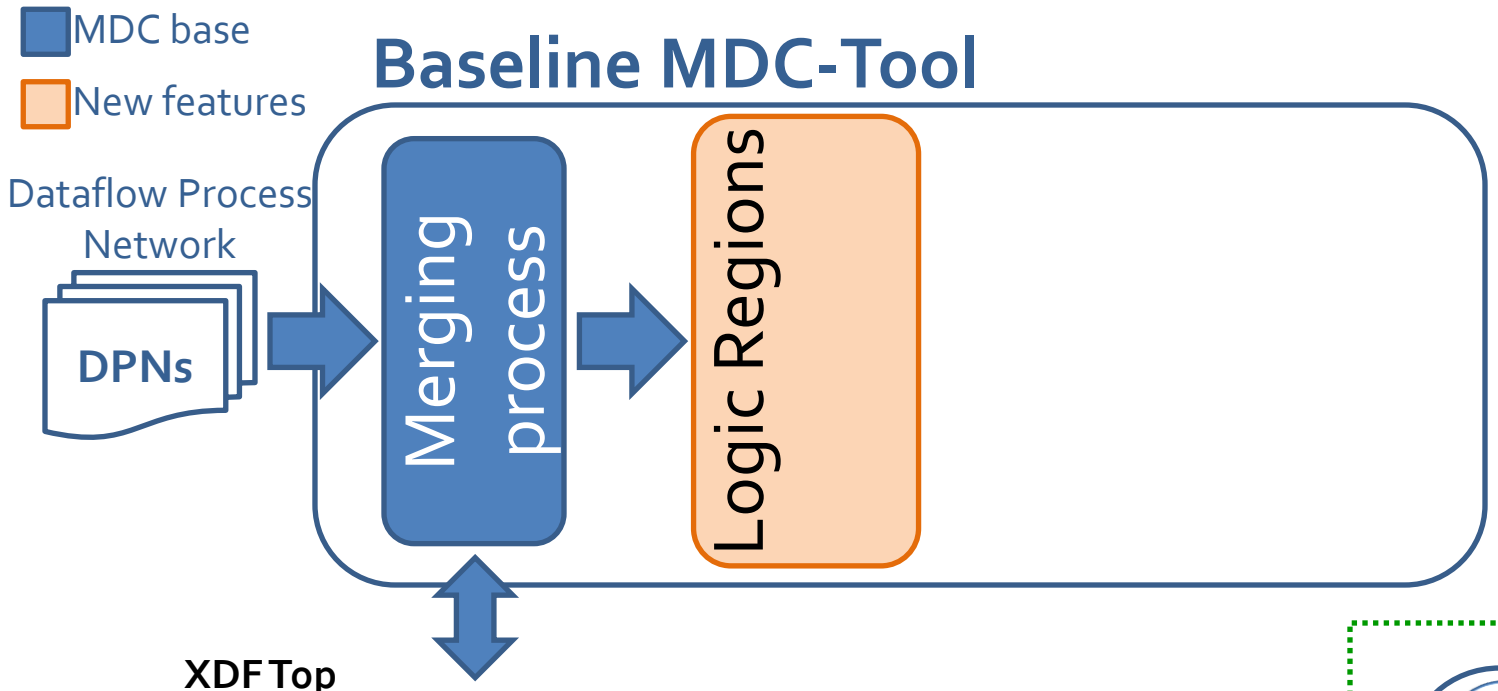




Automated Power Gating

Logic Regions Identification



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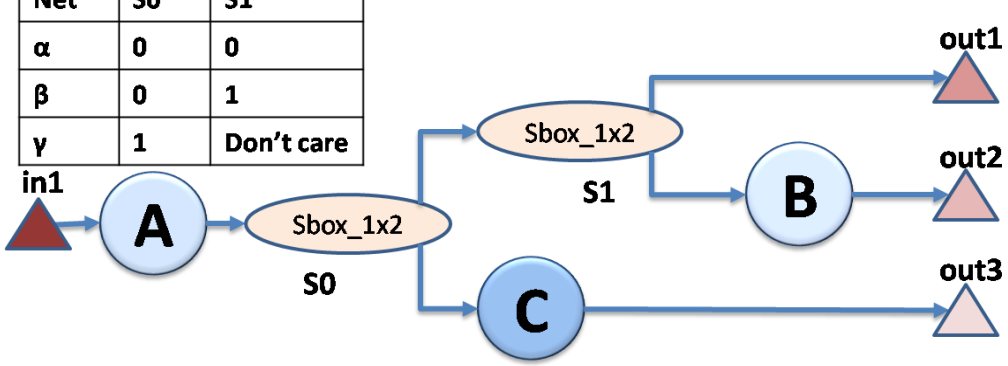
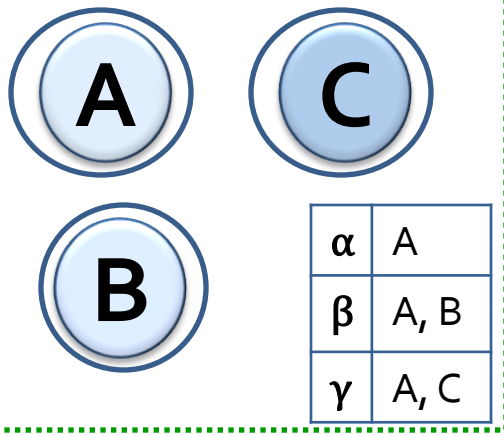
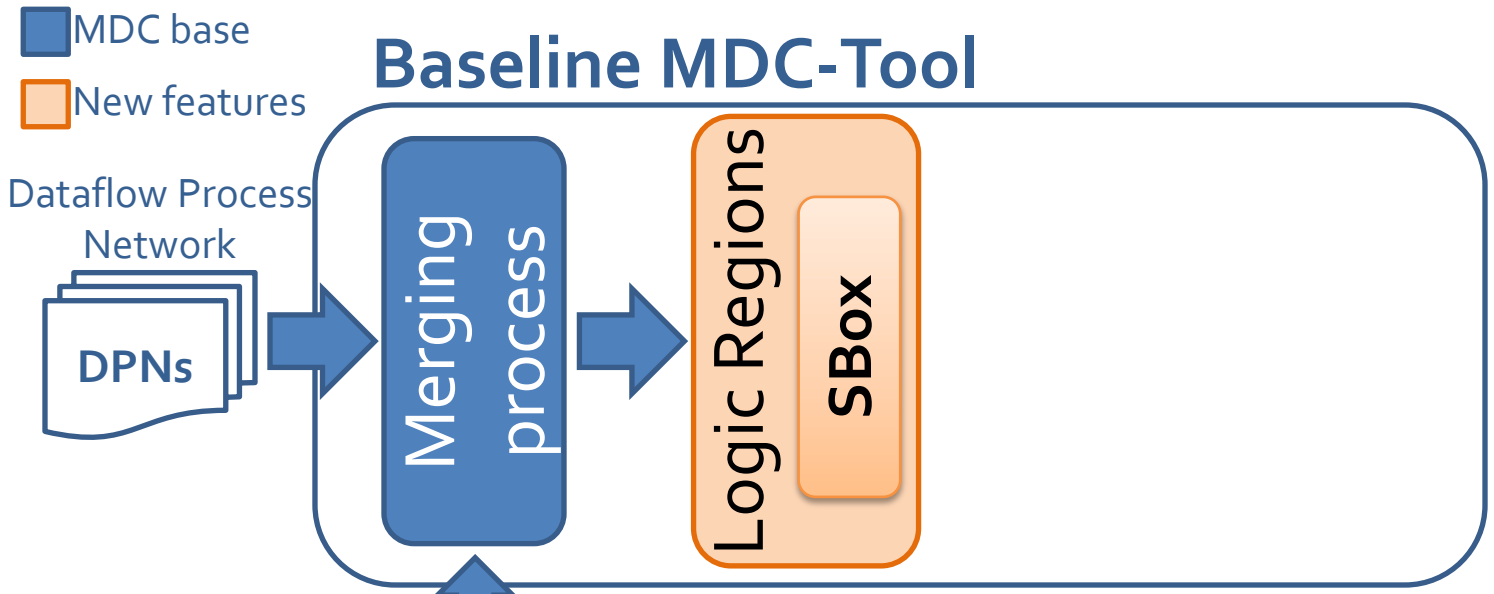




Automated Power Gating

Logic Regions Identification



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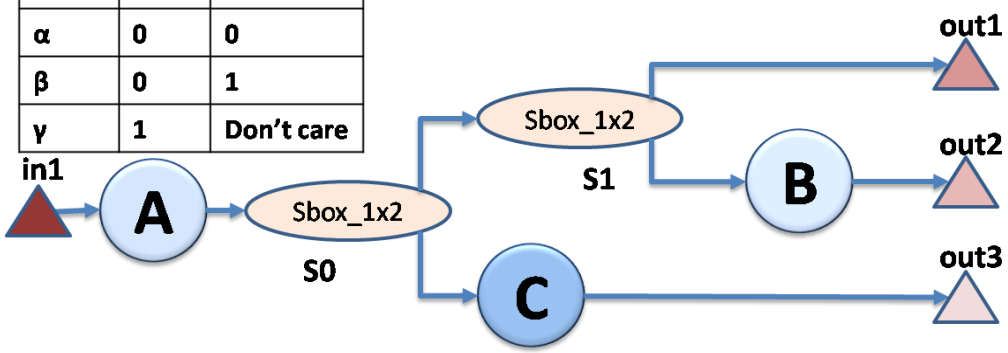

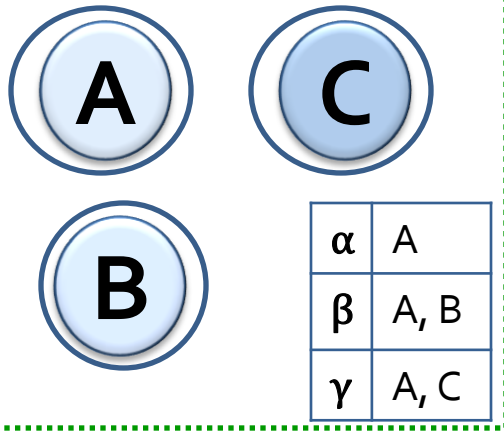

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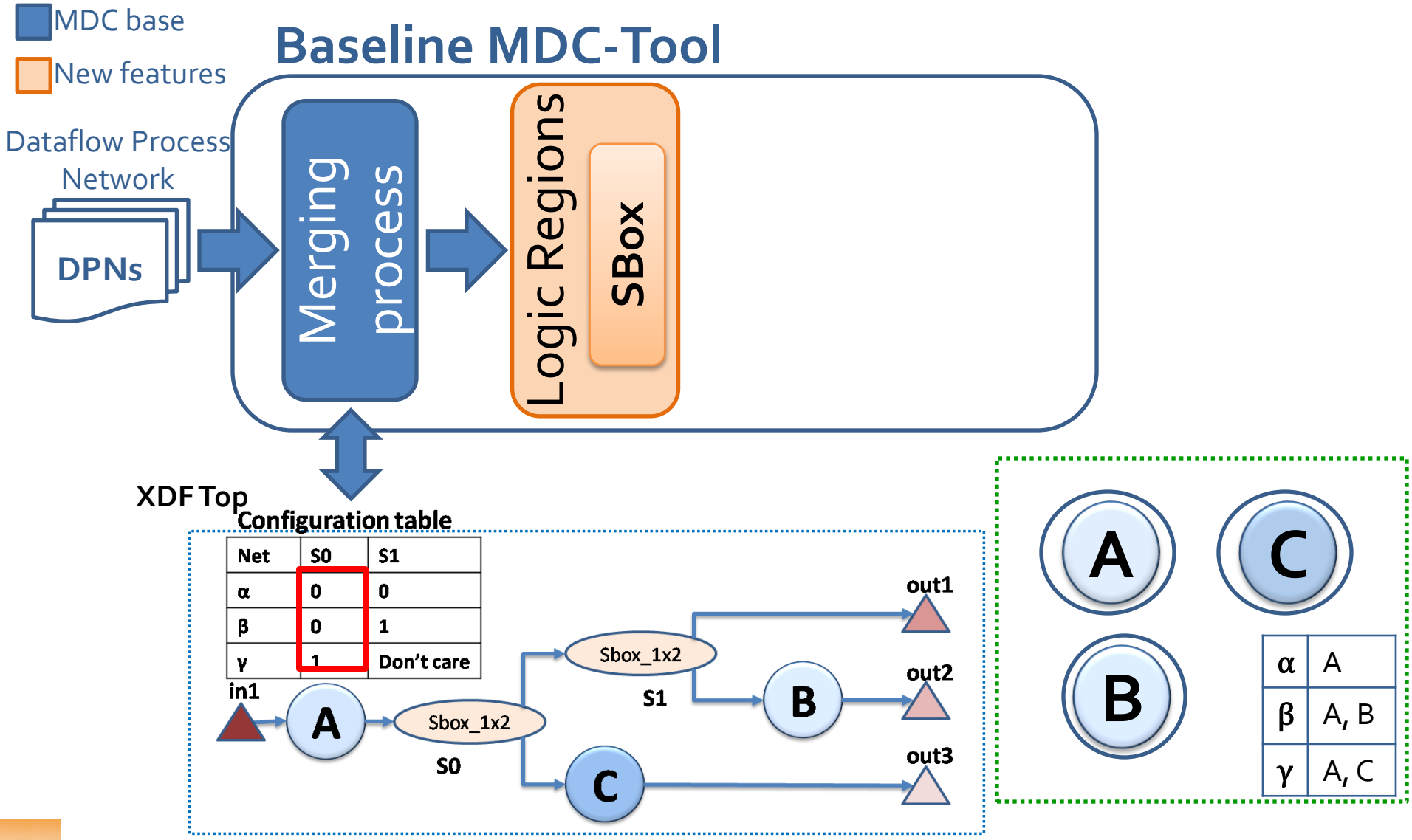

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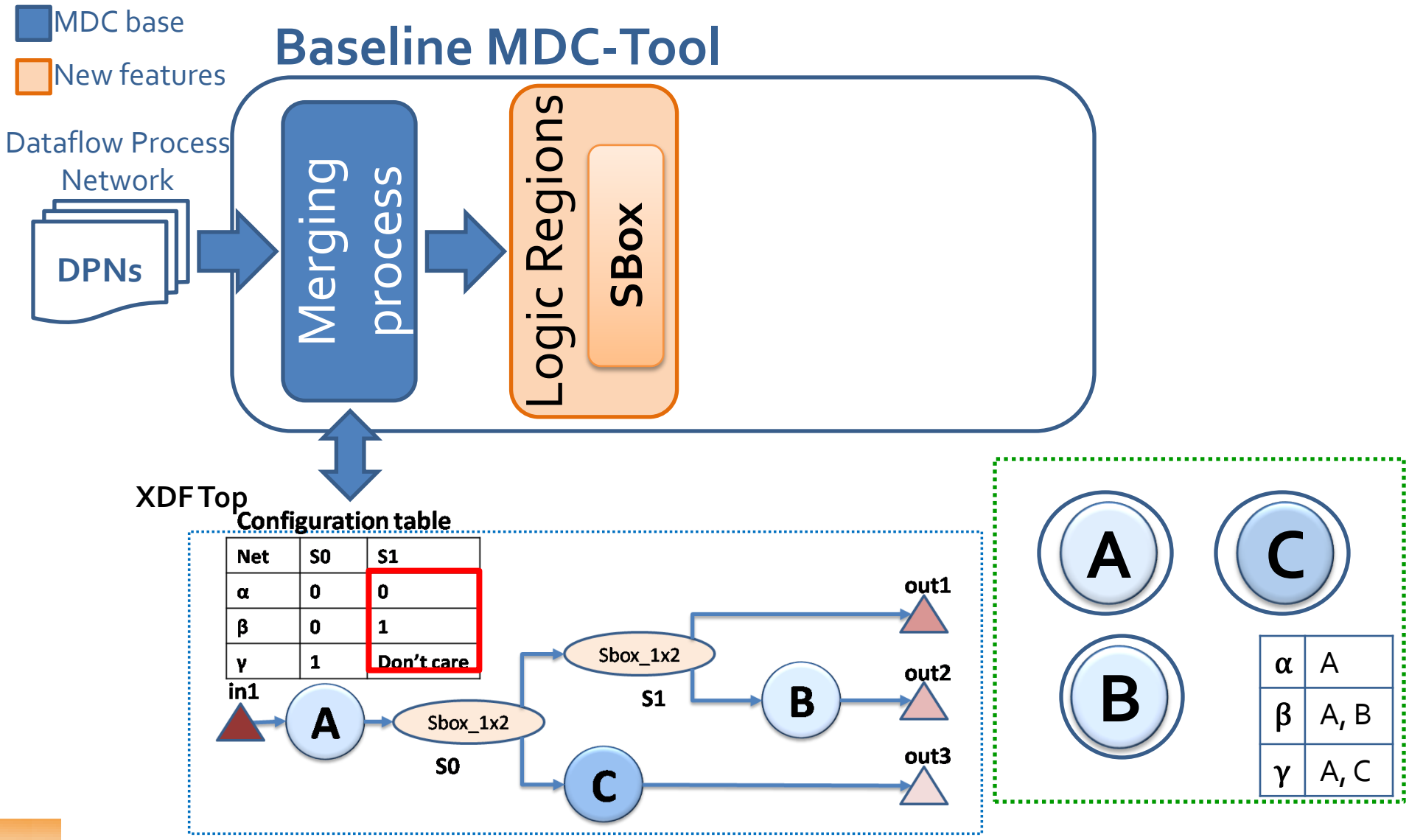

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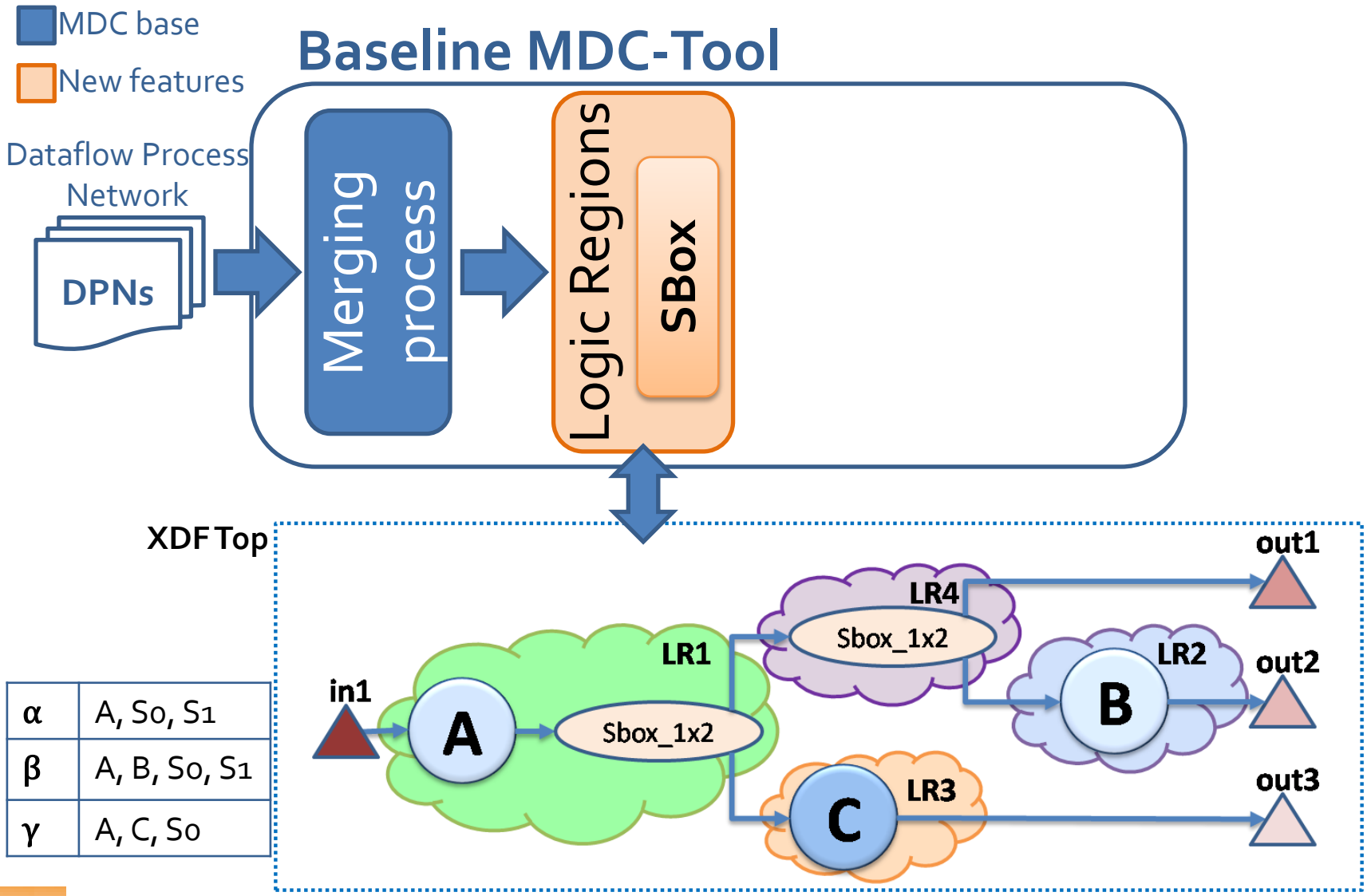

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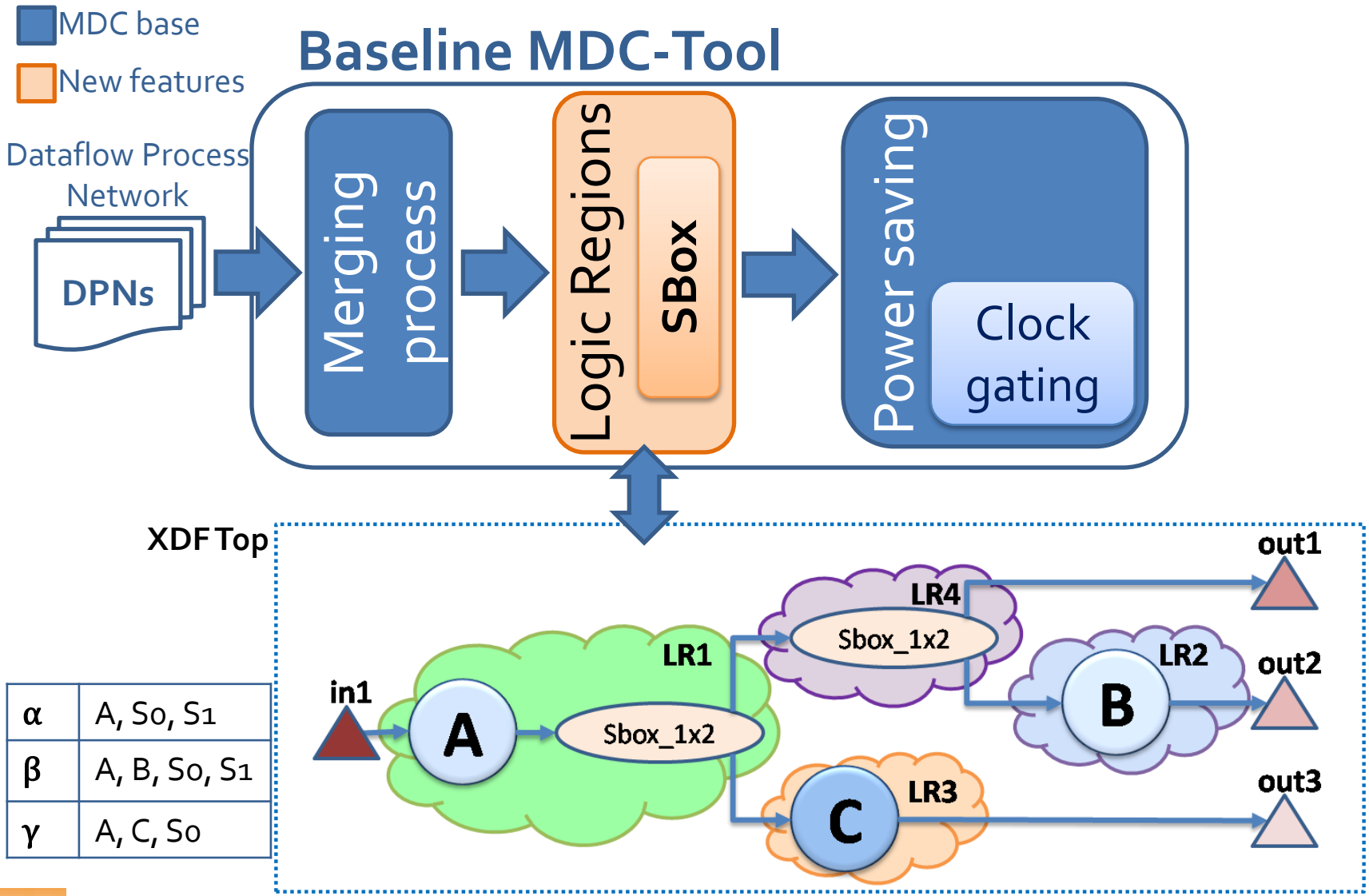

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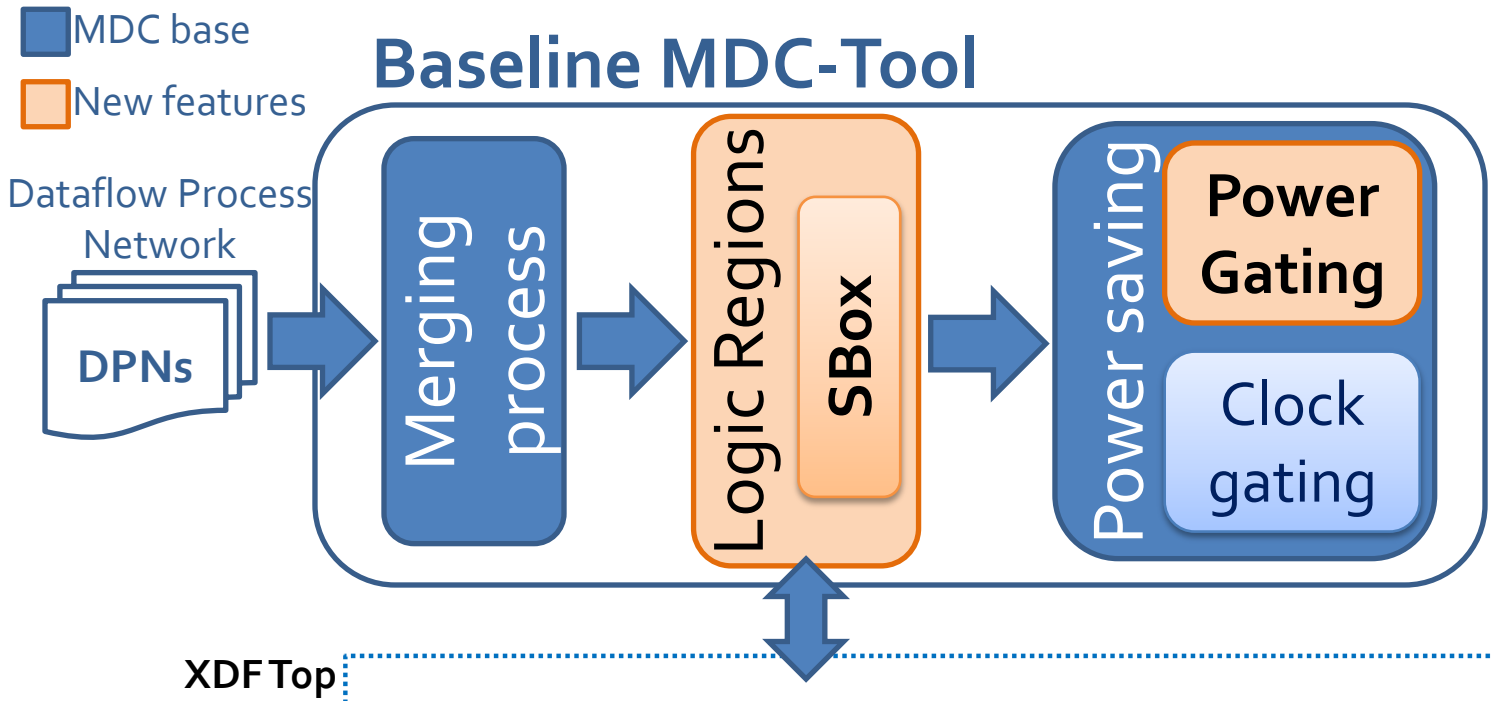

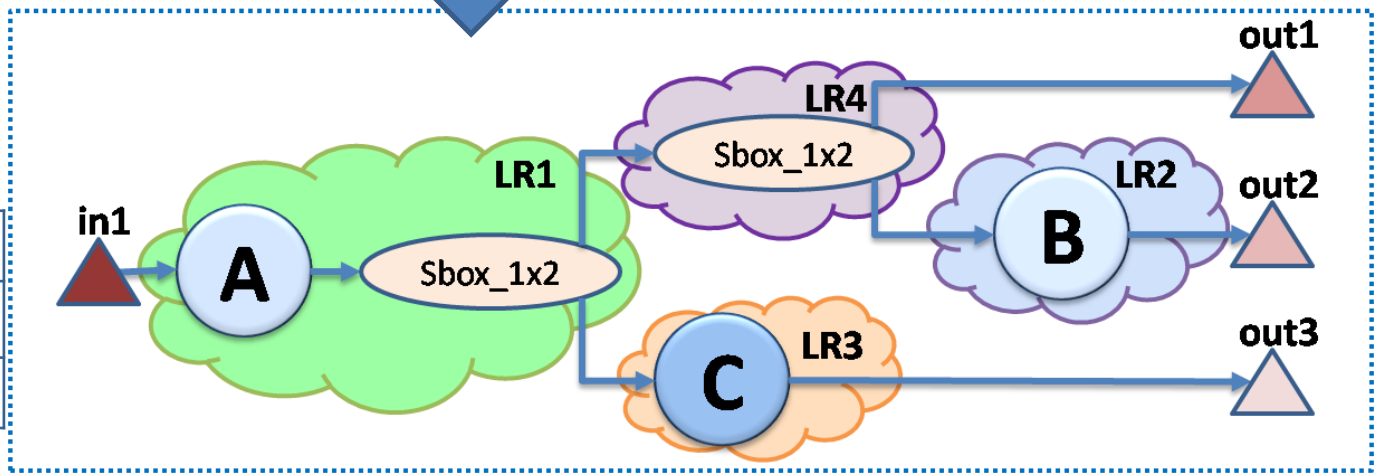

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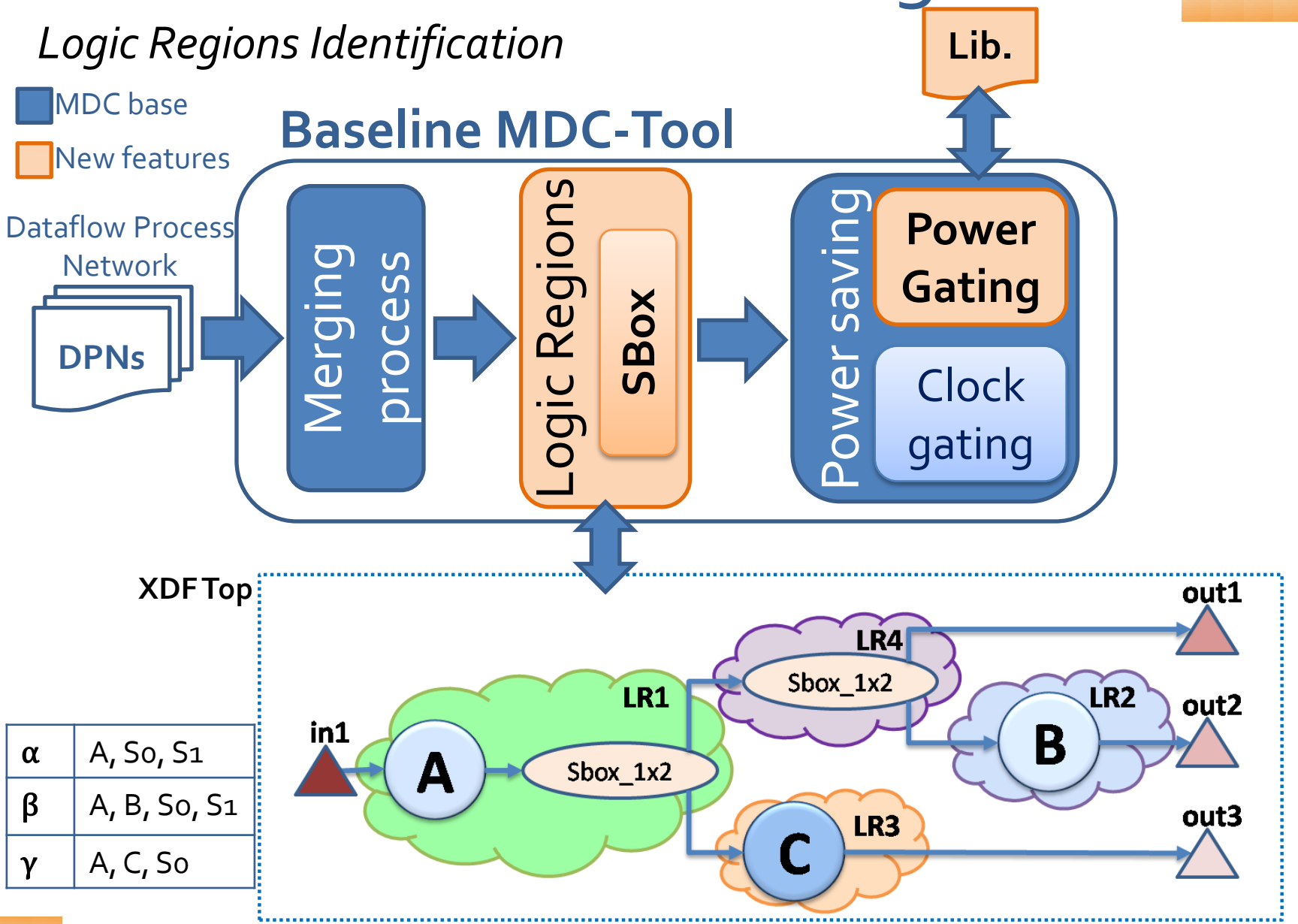

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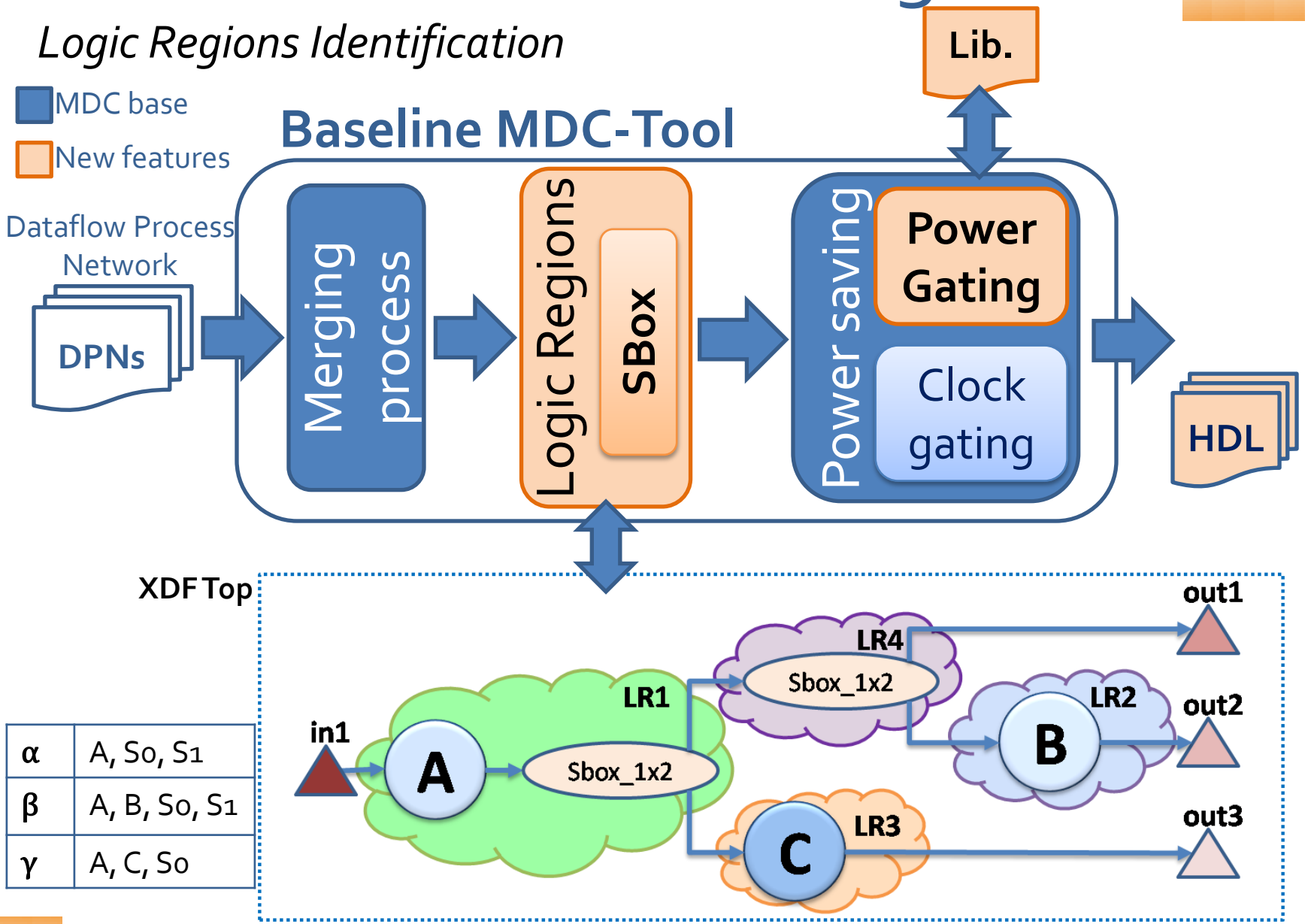

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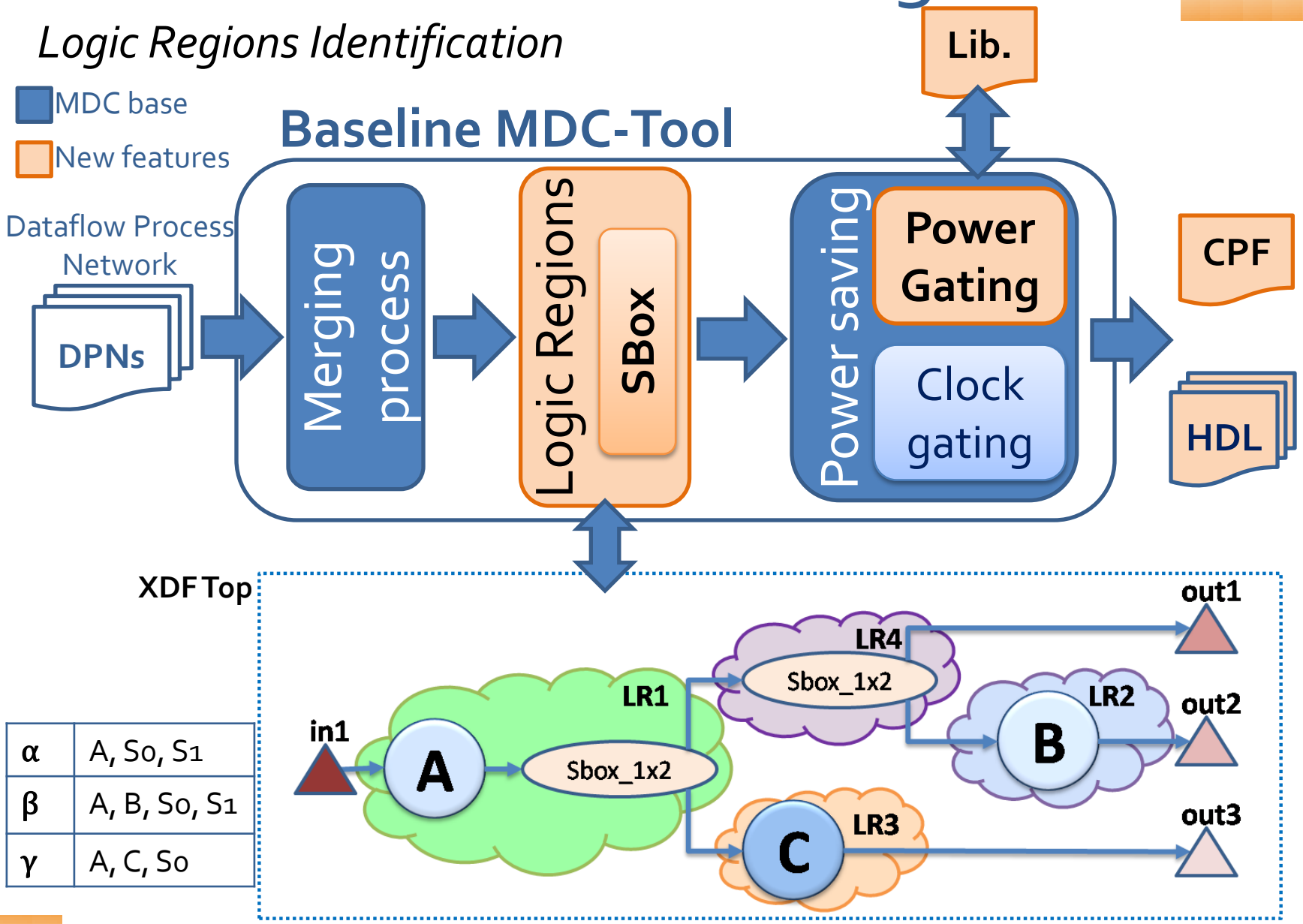

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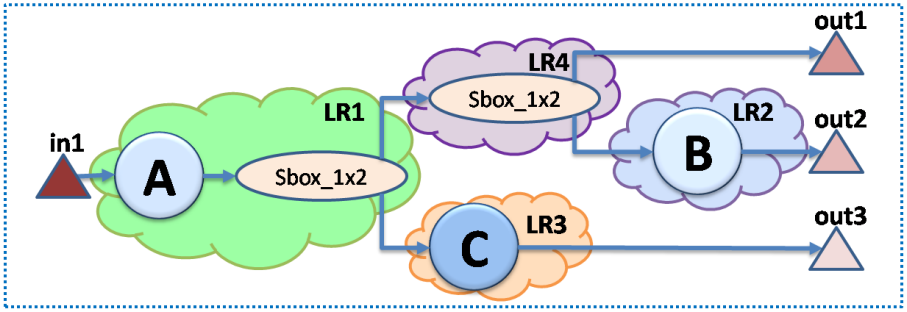
Automated Power Gating

Power Gating Implementation



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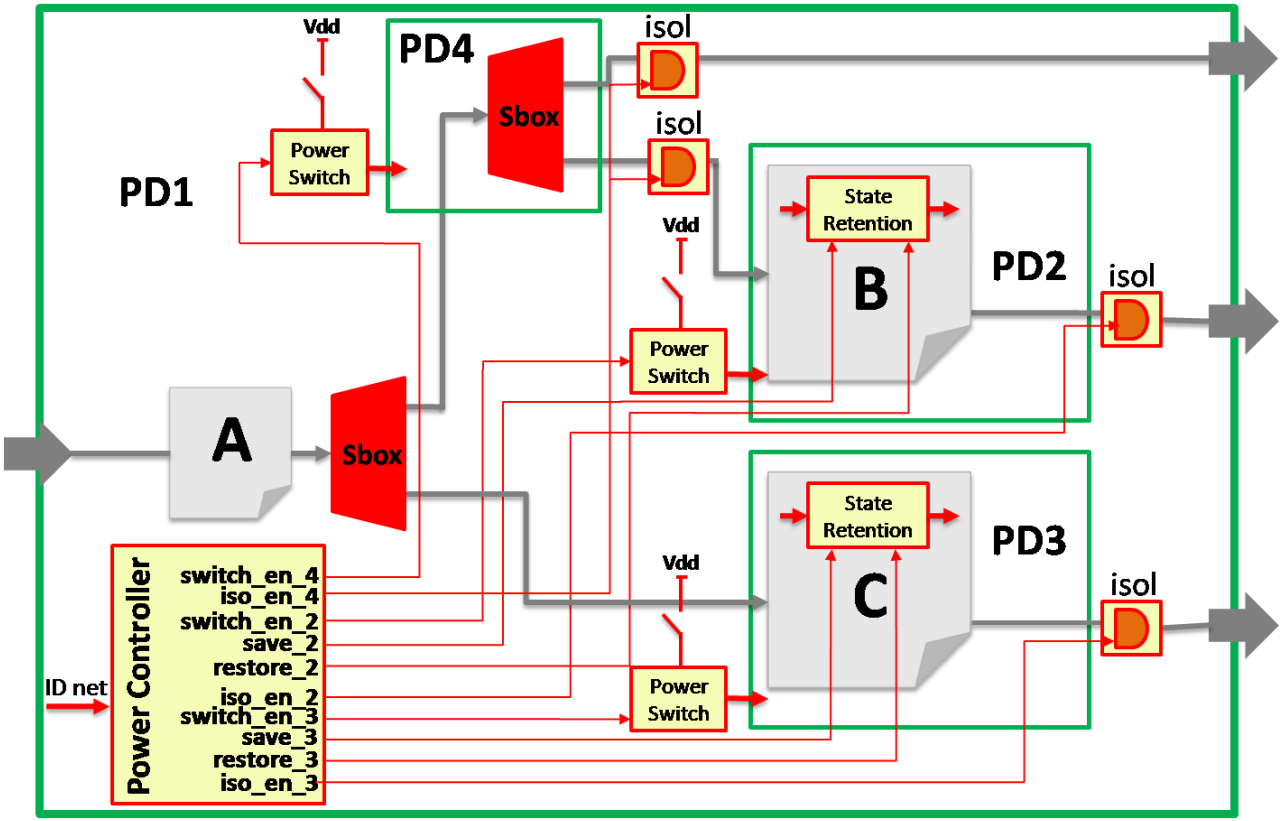

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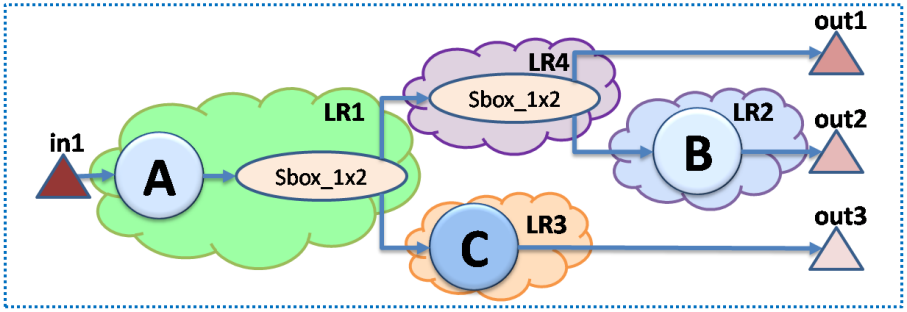

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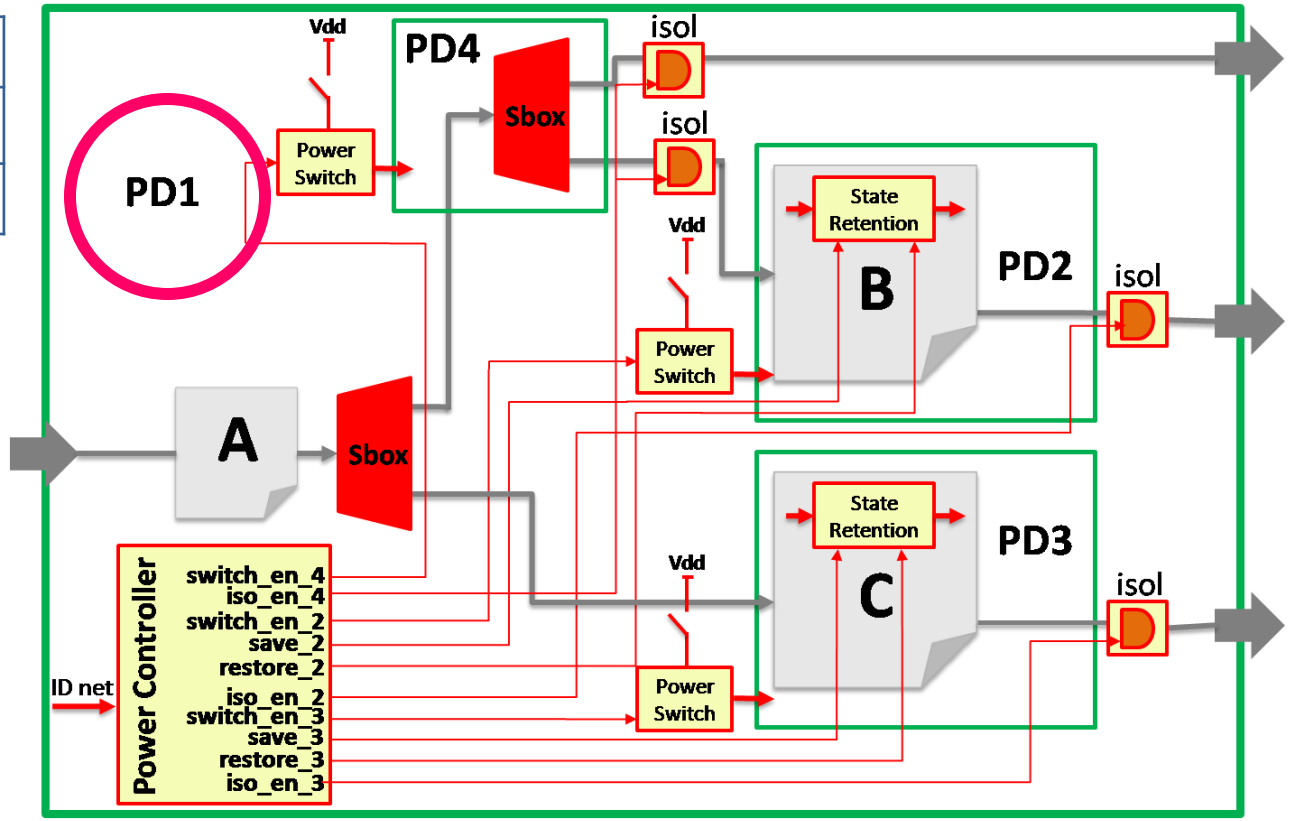

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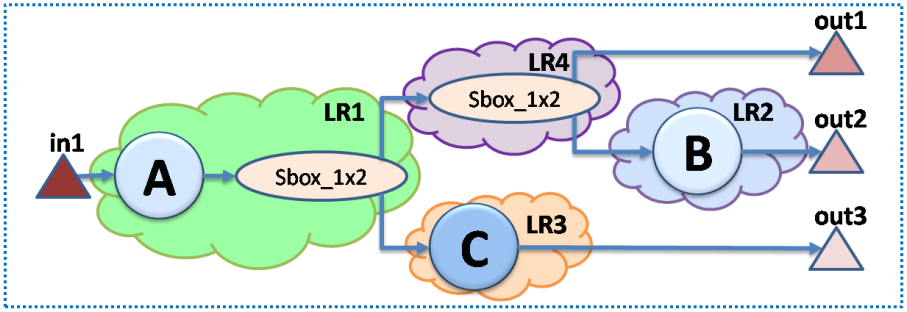

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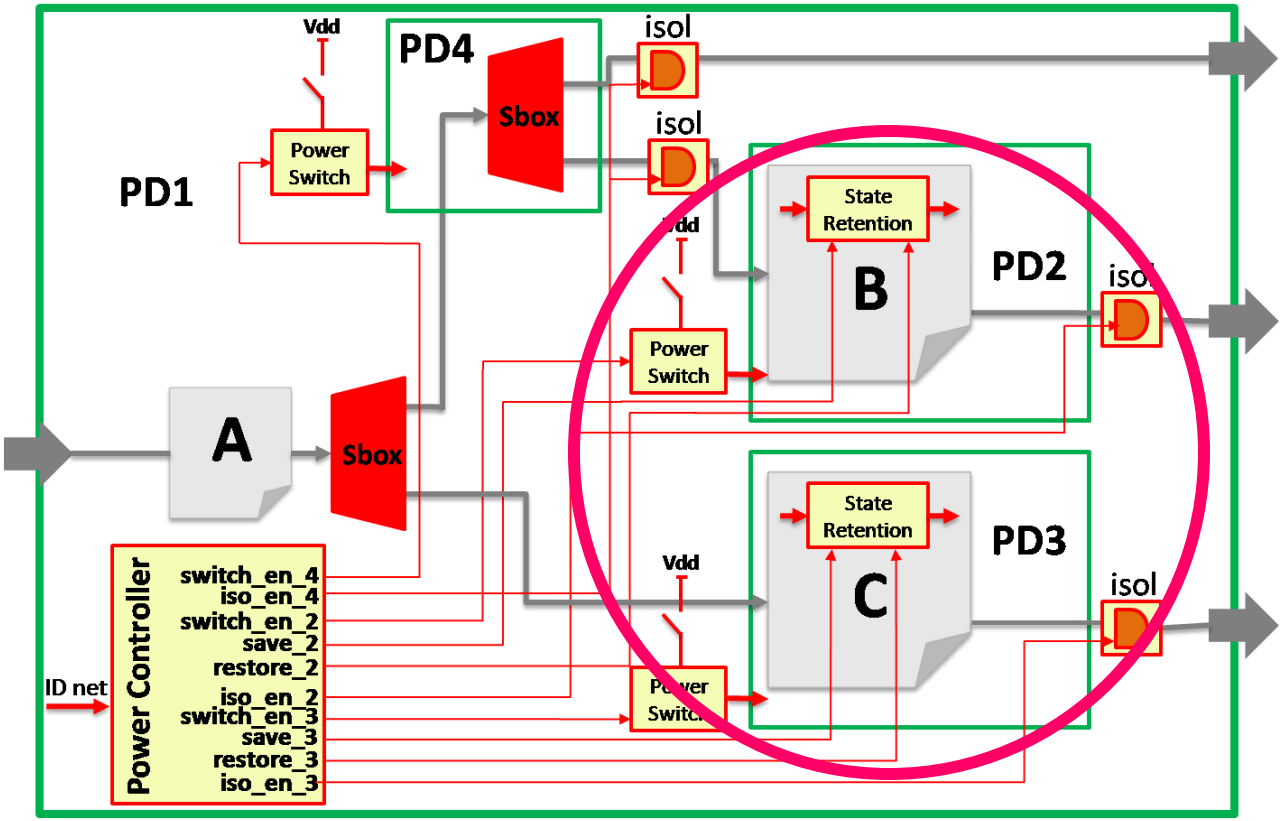

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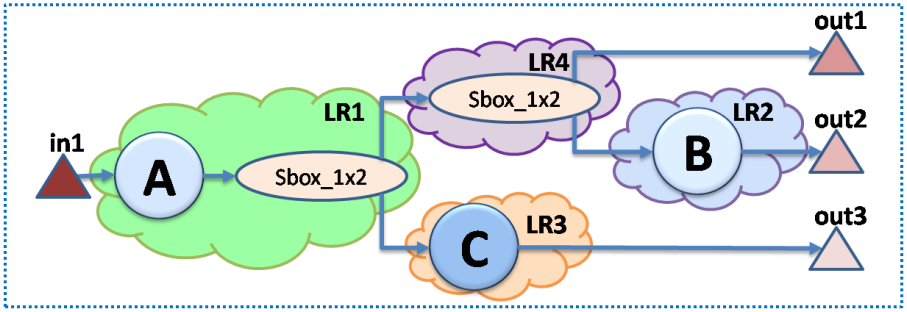

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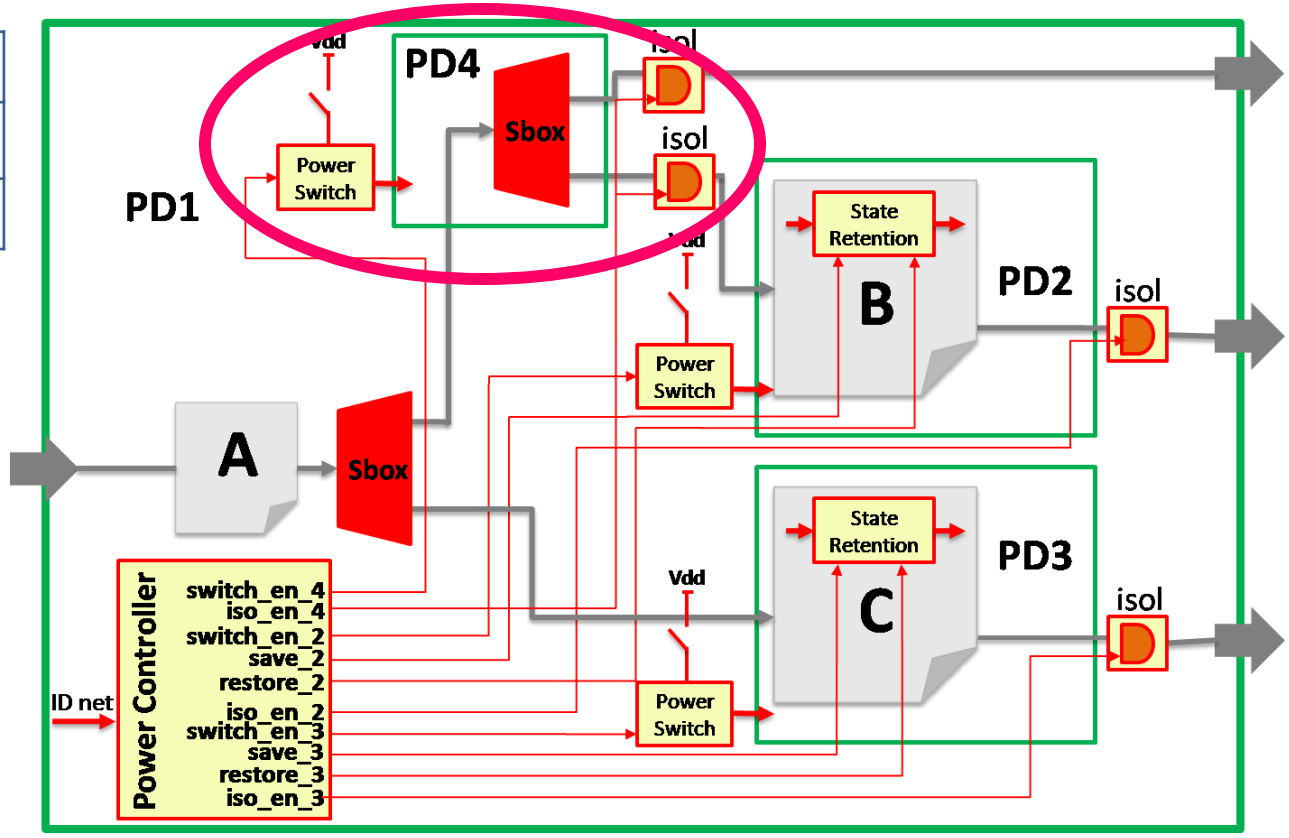

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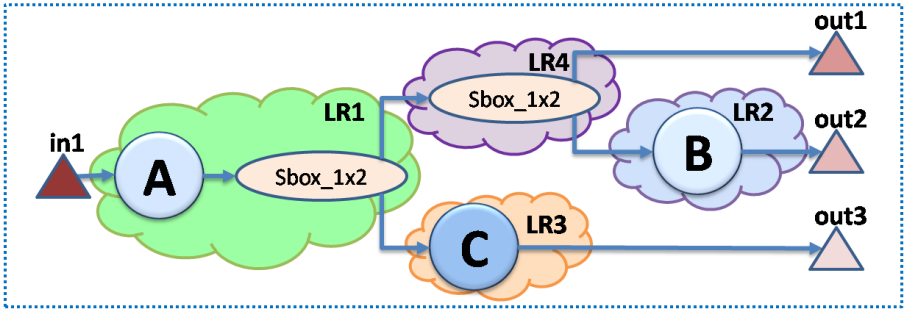

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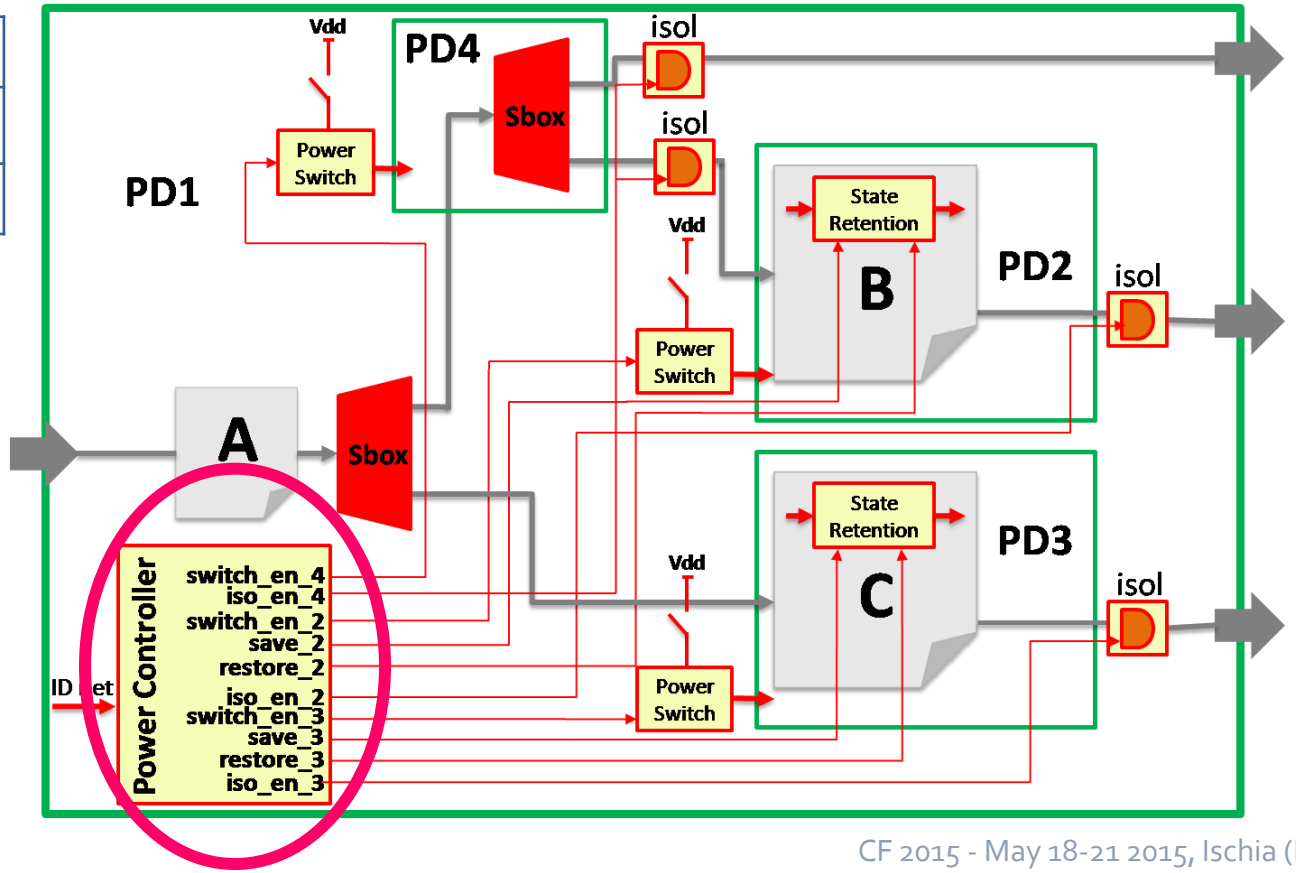
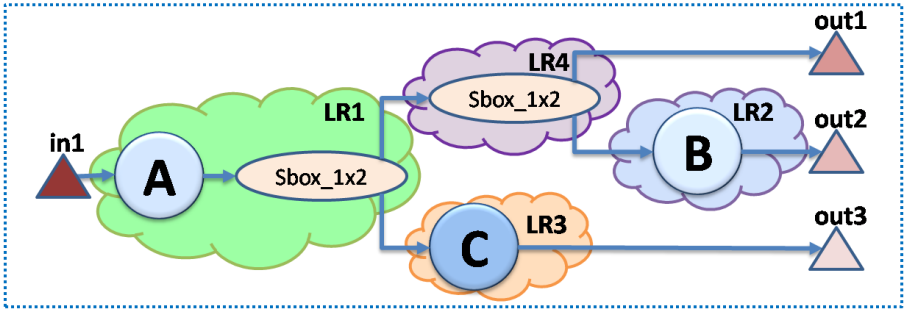


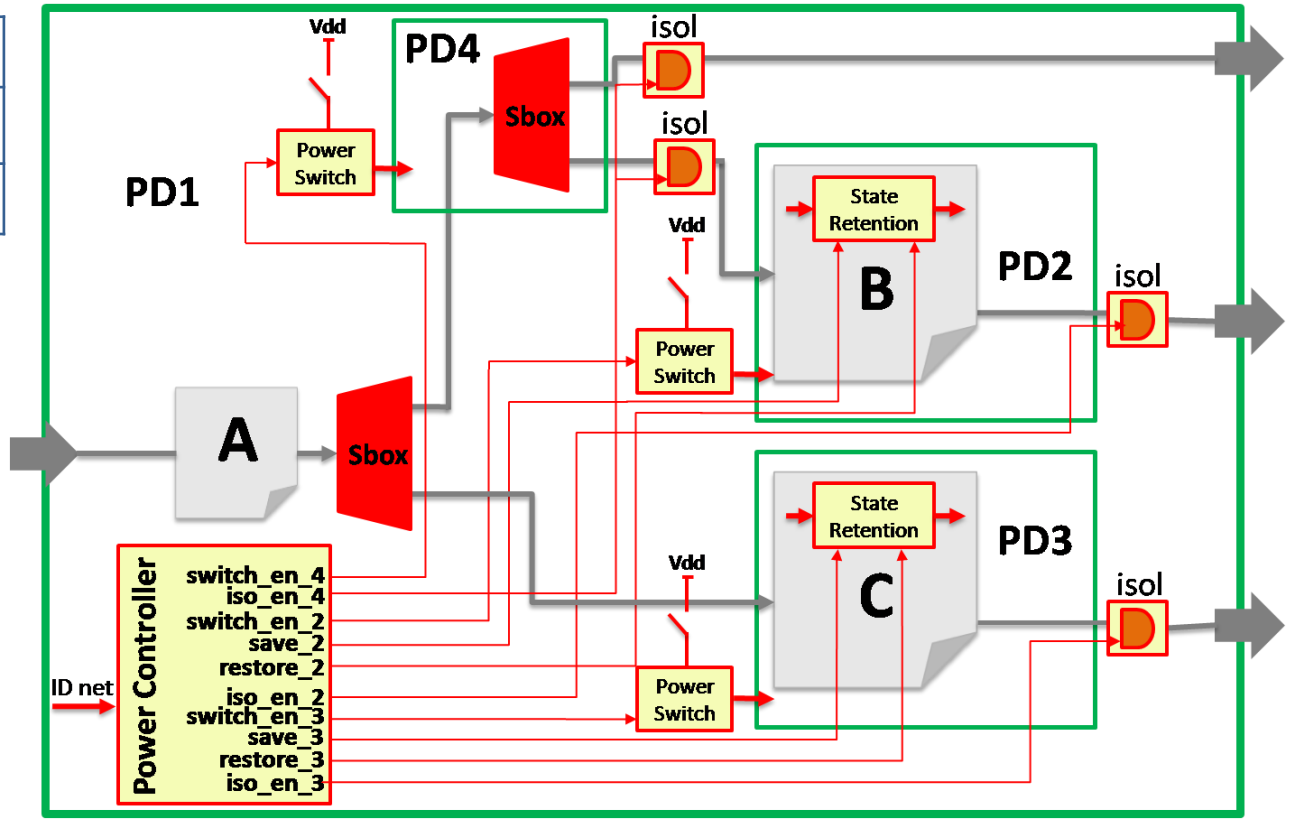
Automated Power Gating

Power Gating Implementation



Network	Power Modes	Power Domains
α	PM1	PD1, PD4
β	PM2	PD1, PD2, PD4
γ	PM3	PD1, PD3

α	A, So, S1
β	A, B, So, S1
γ	A, C, So



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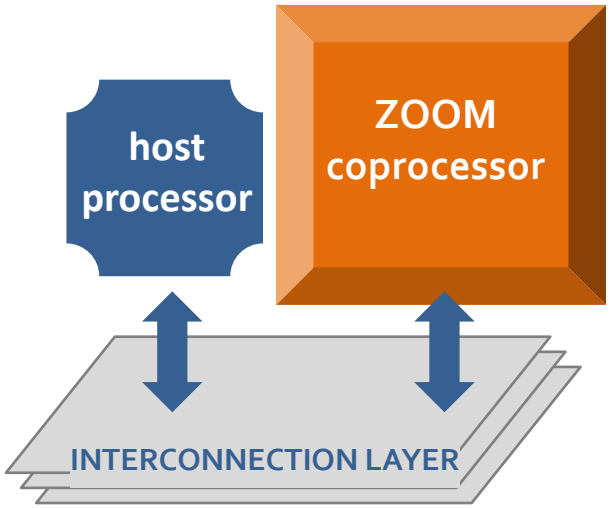
Performance Assessment

Design Under Test: ASIC 90nm technology

APPLICATION	# KERNEL	#ACTORS	# SBOXES	#PDs
zoom	7	33	51	19



Performance Assessment

Design Under Test: ASIC 90nm technology

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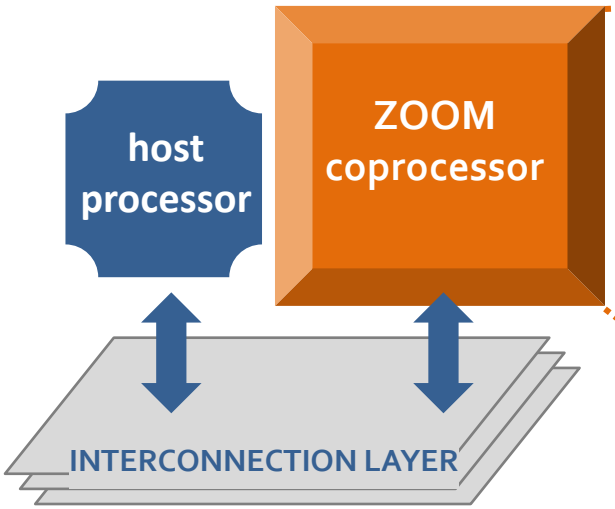
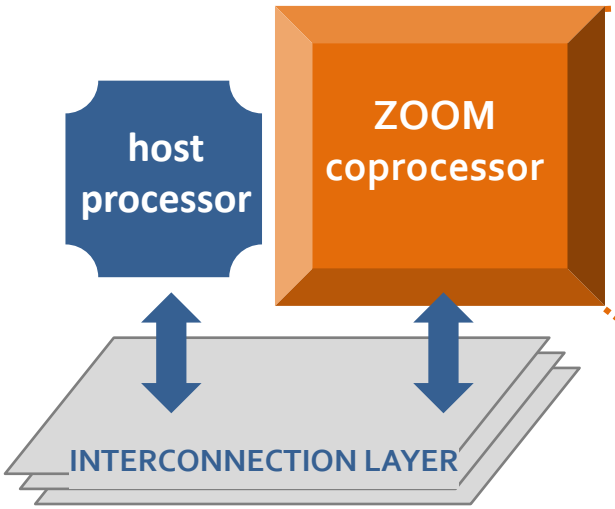


DPN	#ACTORS	#PDs	#OCC
Min-Max	1	7	1050
Abs	1	7	3150
Sbwlabel	17	10	2722
Median	9	7	1069
Chgb	7	9	3072
Cubic	10	6	1070
Cubic_Conv	6	7	408

Performance Assessment

Design Under Test: ASIC 90nm technology

APPLICATION	# KERNEL	#ACTORS	# SBOXES	#PDs
zoom	7	33	51	19



DPN	#ACTORS	#PDs	#OCC
Min-Max	1	7	1050
Abs	1	7	3150
Sbwlabel	17	10	2722
Median	9	7	1069
Chgb	7	9	3072
Cubic	10	6	1070
Cubic_Conv	6	7	408

Performance Assessment

Experimental Results: single kernels result

DPN	#ACTORS	#PDs	#OCC
Min-Max	1	7	1050
Abs	1	7	3150
Sbwlabel	17	10	2722
Median	9	7	1069
Chgb	7	9	3072
Cubic	10	6	1070
Cubic_Conv	6	7	408

Performance Assessment

Experimental Results: single kernels result

Zoom → MDC baseline

Zoom_cg → MDC clock gating methodology

Zoom_pg → proposed power gating methodology

DPN	#ACTORS	#PDs	#OCC
Min-Max	1	7	1050
Abs	1	7	3150
Sbwlabel	17	10	2722
Median	9	7	1069
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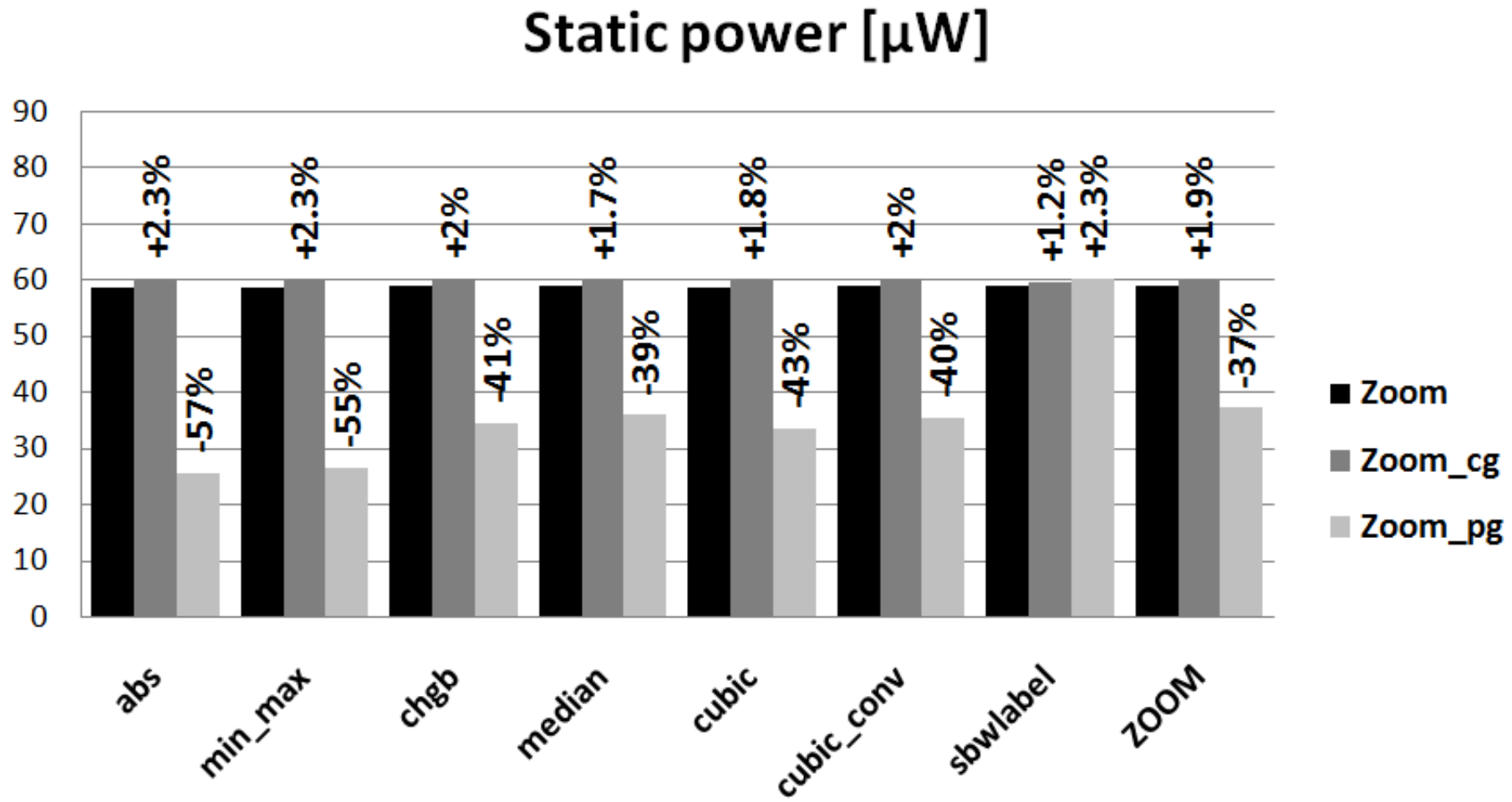
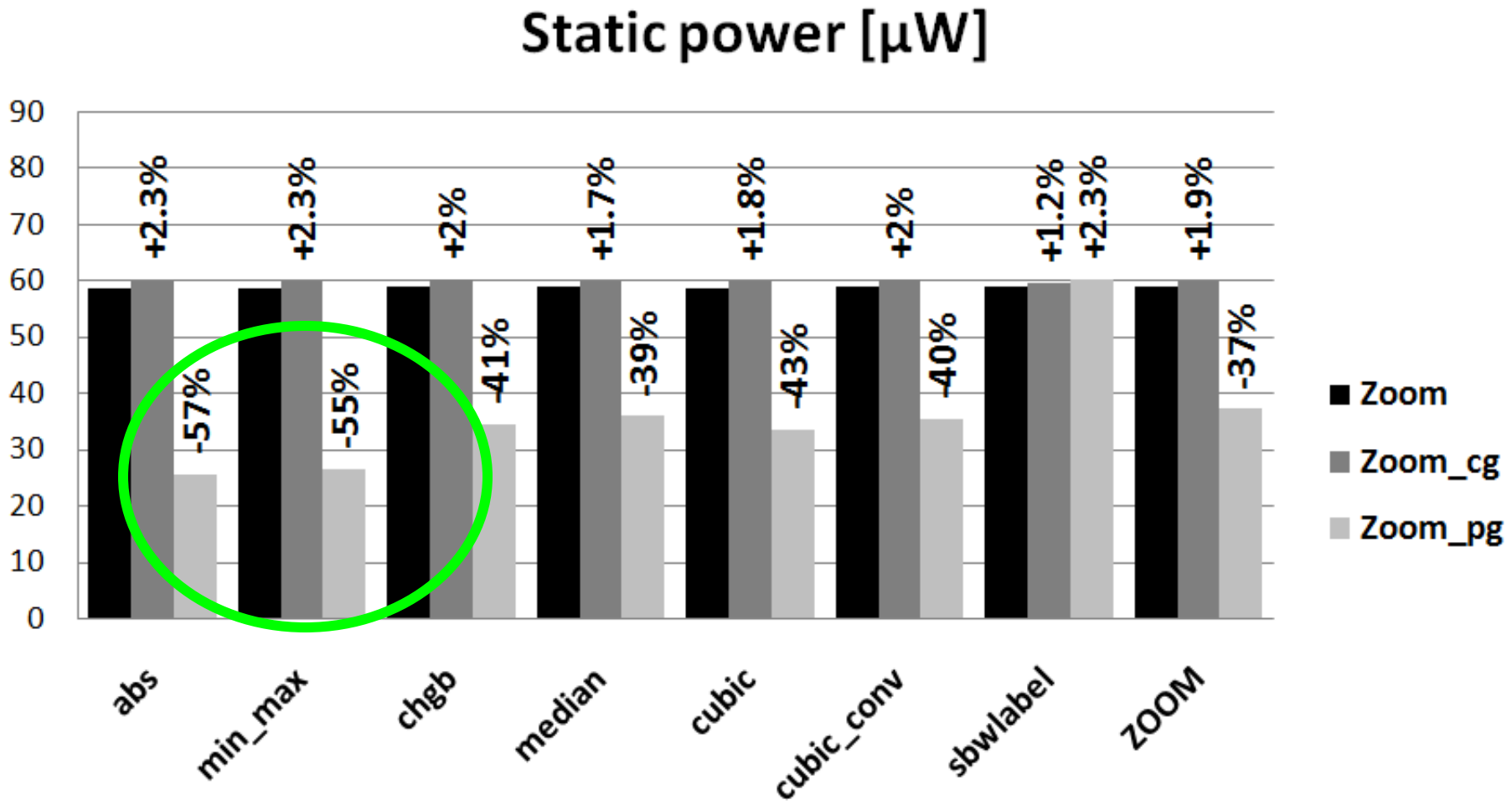
Performance Assessment

Experimental Results: single kernels result



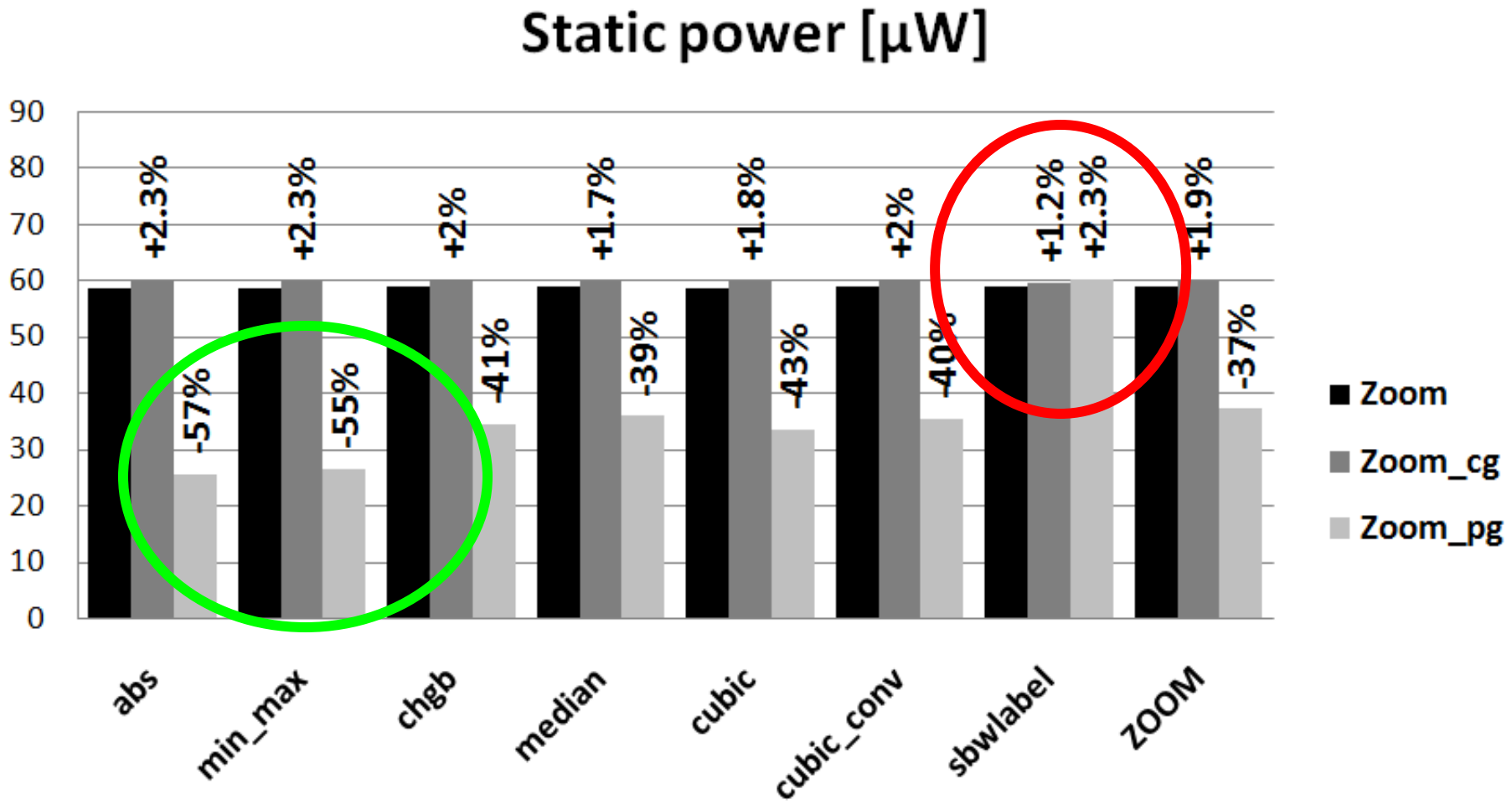
Performance Assessment

Experimental Results: single kernels result



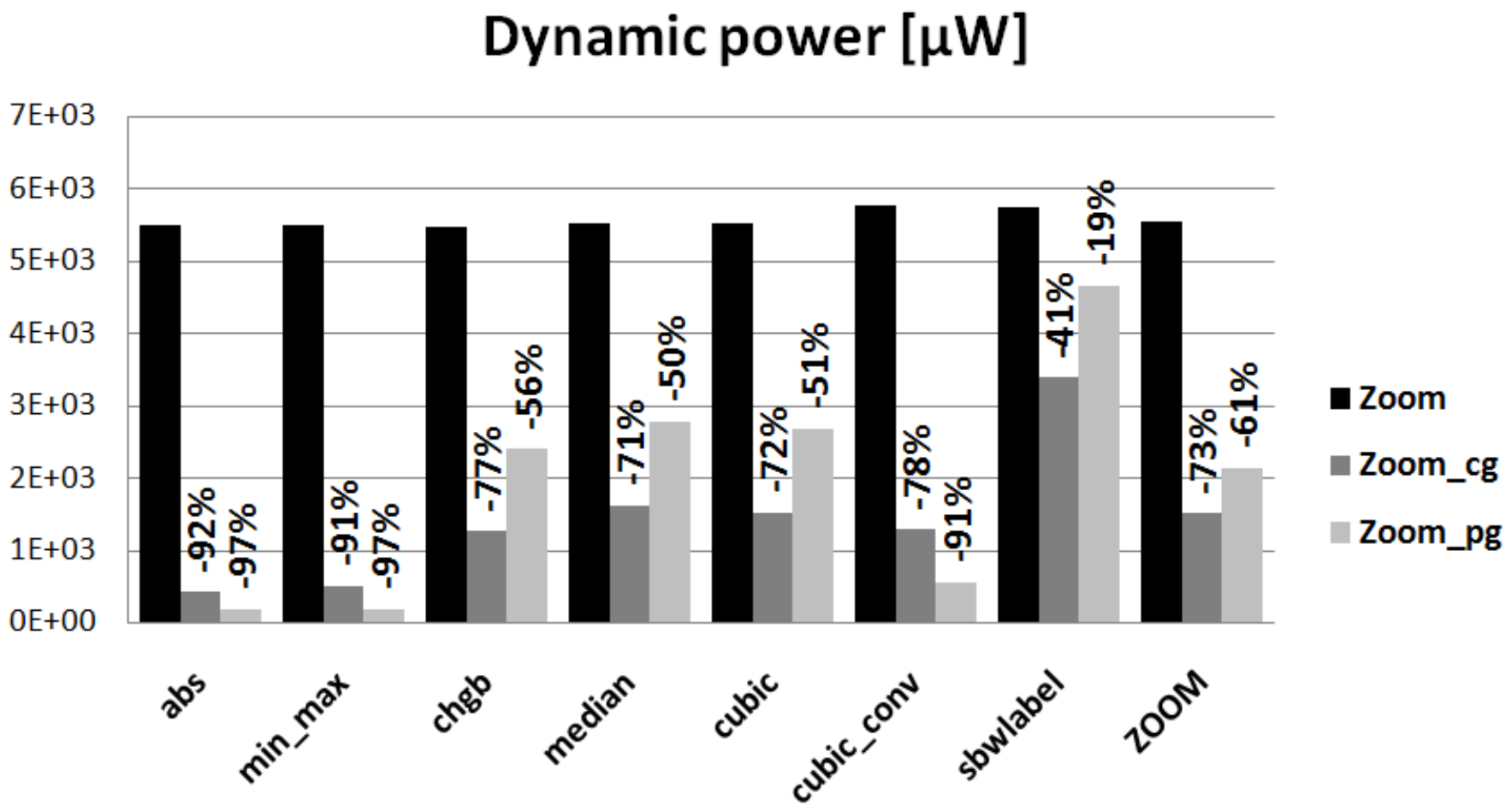
Performance Assessment

Experimental Results: single kernels result



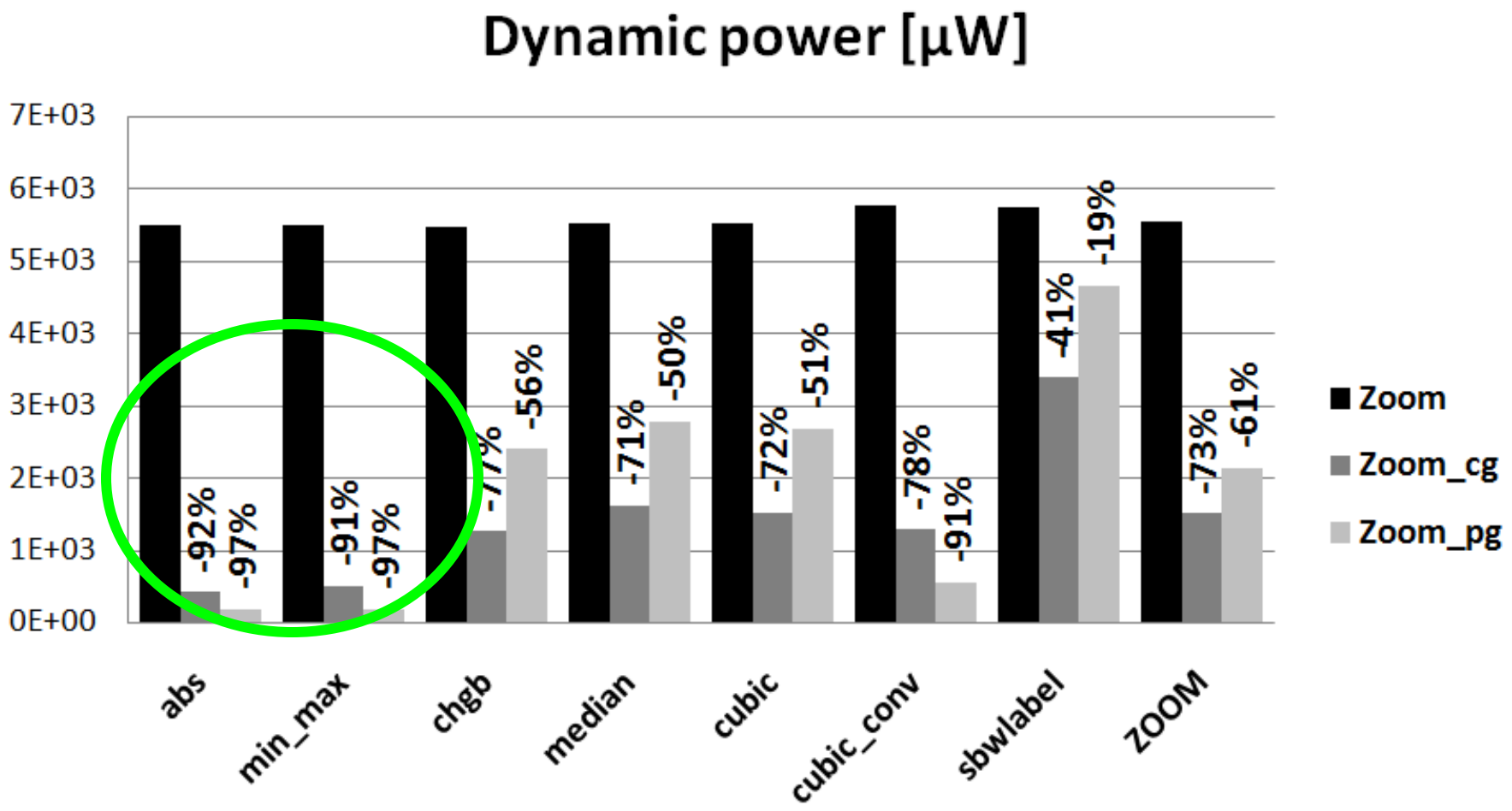
Performance Assessment

Experimental Results: single kernels result



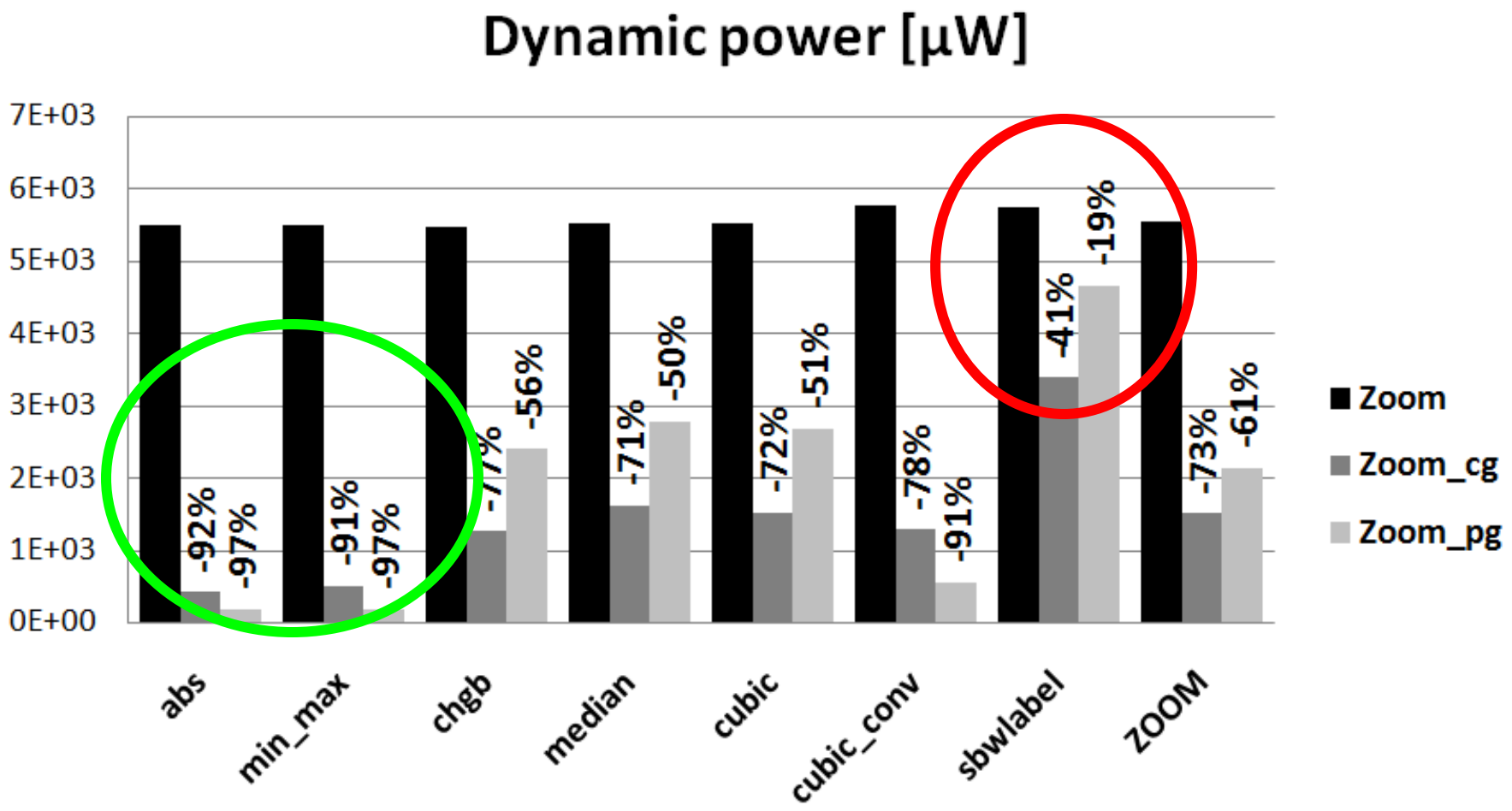
Performance Assessment

Experimental Results: single kernels result



Performance Assessment

Experimental Results: single kernels result



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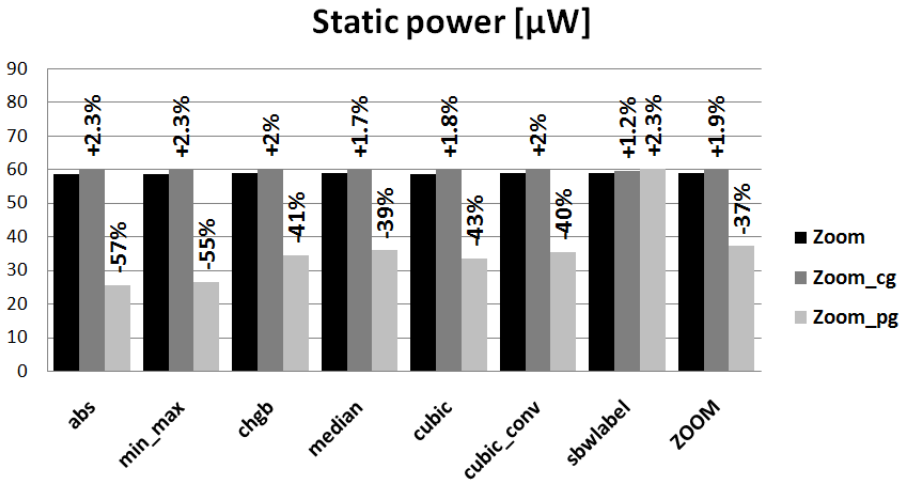

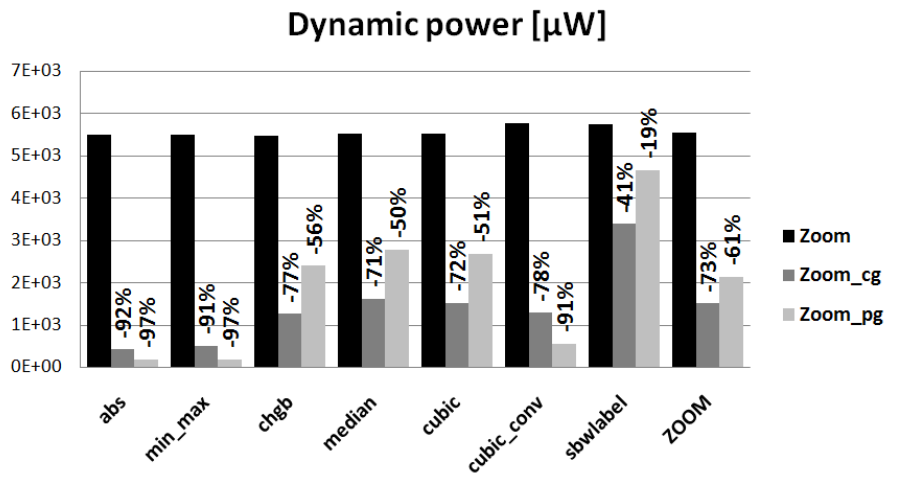

DPN	#ACTORS	#PDs	#OCC
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Abs	1	7	3150
Sbwlabel	17	10	2722
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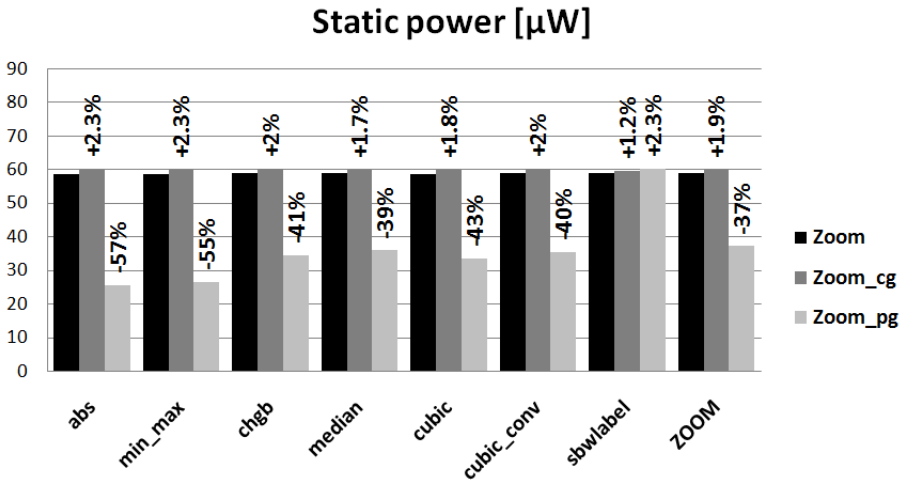
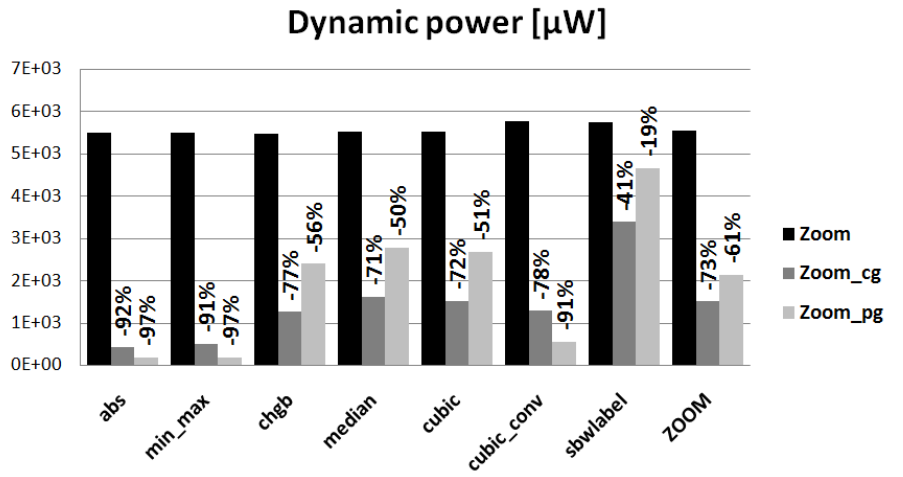
Performance Assessment

Experimental Results: single kernels result





DPN	#ACTORS	#PDs	#OCC
Min-Max	1	7	1050
Abs	1	7	3150
Sbwlabel	17	10	2722
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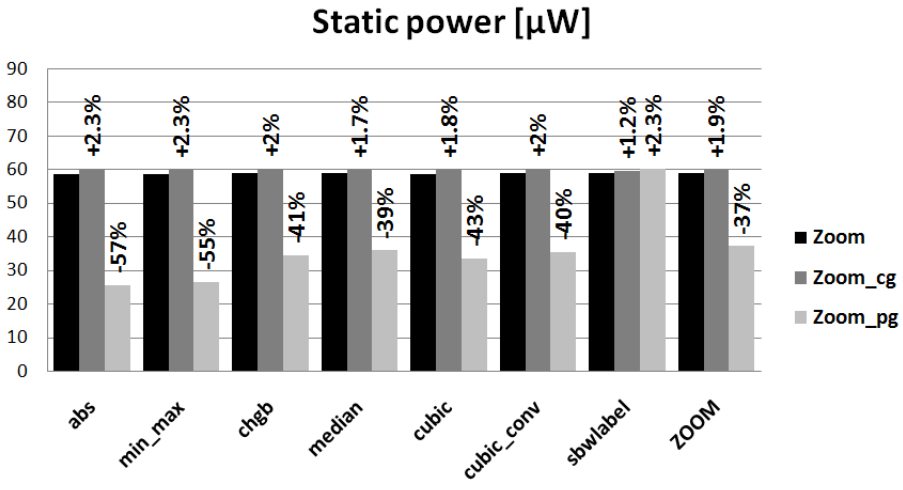
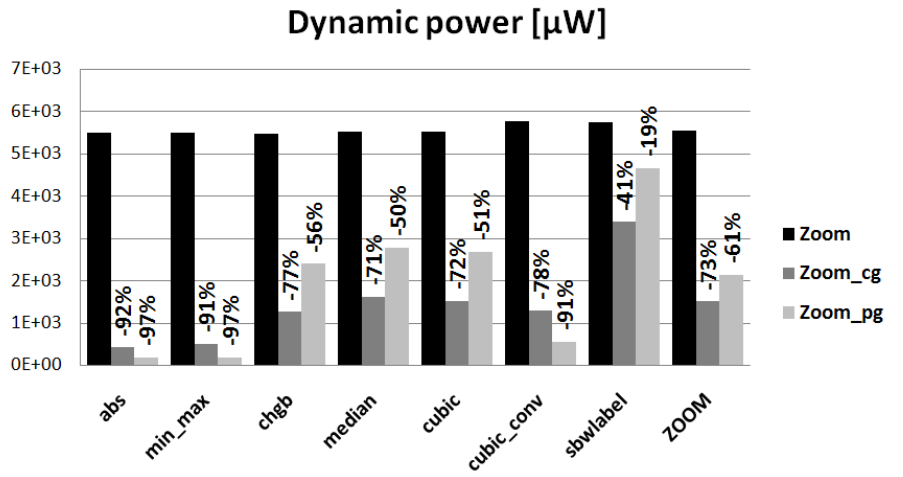
Performance Assessment

Experimental Results: single kernels result





More than 50%
of the design is
ACTIVE

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Sbwlabel	17	10	2722
Median	9	7	1069
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Performance Assessment

Experimental Results: general results

DESIGN	AREA		POWER	
	[µm2]	%	[µW]	%
Zoom	118271	----	5610	----
Zoom_cg	118695	+0.36	1557	-72.25
Zoom_pg	224293	+89.9	2176	-61.21

cg = with the MDC high-level clock gating
pg= with the proposed high-level power gating

Performance Assessment

Experimental Results: general results

DESIGN	AREA		POWER	
	[µm2]	%	[µW]	%
Zoom	118271	----	5610	----
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Area + 89.9% ☹

Performance Assessment

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Saving pg < Saving cg 😐?

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Data Dependent !

A different example!

DPN	#ACTORS	#OCC	#OCC
Min-Max	1	1050	**341**
Abs	1	3150	**15142**
Sbwlabel	17	2722	**1496**
Median	9	1069	**1253**
Chgb	7	3072	**70045**
Cubic	10	1070	**966**
Cubic_Conv	6	408	**3072**

Performance Assessment

Experimental Results: general results

DESIGN	AREA		POWER	
	[µm2]	%	[µW]	%
Zoom	118271	----	5610	----
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A different example!

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Median	9	1069	**1253**
Chgb	7	3072	**70045**
Cubic	10	1070	**966**
Cubic_Conv	6	408	**3072**

New Zoom Test

DESIGN	POWER	
	[µW]	%
Zoom	5544	----
Zoom_cg	581	-89.51
Zoom_pg	**400**	**-92.77**

Performance Assessment

Experimental Results: general results

DESIGN	AREA		POWER	
	[µm2]	%	[µW]	%
Zoom	118271	----	5610	----
Zoom_cg	118695	+0.36	1557	-72.25
Zoom_pg	224293	+89.9	2176	-61.21

Area + 89.9% ☹

Power -61.21% ☺

Saving pg < Saving cg 😐?

Static << Dynamic !

Data Dependent !

Carefully choose the strategy to implement according to the overall scenario characteristics.

Zoom_cg	581	-89.51
Zoom_pg	**400**	**-92.77** ☺

Cubic	10	1070	**966**
Cubic_Conv	6	408	**3072**

Outline

- Introduction
  - Increasing Complexity
  - Problem Statement
- Background
  - Dataflow Model of Computation
  - Coarse-Graine Reconfiguration: Multi-Dataflow Composer Tool - MDC
  - Power Management
- Automated Power Gating Strategy
  - Logic Regions Identification
  - Power Gating Implementation
- Performance Assessment
  - Design Under Test
  - Experimental Results
- Final Remarks and Future Directions

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Final Remarks and Future Directions

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  - provides efficient power-aware architectures
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- Future developments
  - Early stage PDs profiling

Final Remarks and Future Directions

- Power consumption management is a challenging issue in modern embedded system designs
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Final Remarks and Future Directions

- Power consumption management is a challenging issue in modern embedded system designs
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  - implements coarse-grained multi-functional devices
  - provides efficient power-aware architectures
- **MDC now integrates high-level power gating strategy**
- Future developments
  - Early stage PDs profiling
  - Power gating on different logic regions (Exclude Sboxes or small actors)
  - Hybrid clock gating/power gating methodology

Acknowledgements

The research leading to these results has received funding from:

• the Region of Sardinia L.R.7/2007 under grant agreement CRP-18324 [RPCT Project].

• the Region of Sardinia, Young Researchers Grant, POR Sardegna FSE 2007-2013, L.R.7/2007 "Promotion of the scientific research and technological innovation in Sardinia"

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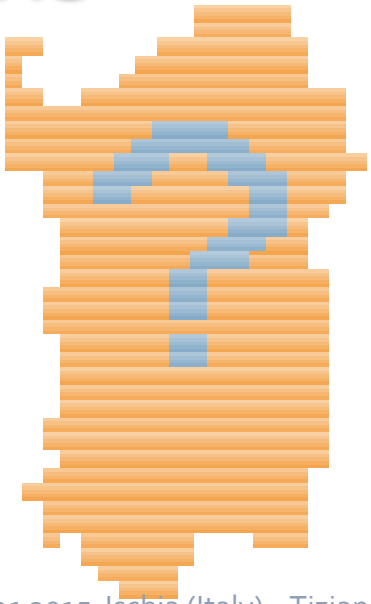
DIEE – Dept. of Electrical and Electronics Eng.
EOLAB - Microelectronics and Bioeng. Lab.

Francesca Palumbo
Università degli Studi di Sassari
PolComIng
Information Engineering Unit

Automated Power Gating Methodology for Dataflow-Based Reconfigurable Systems

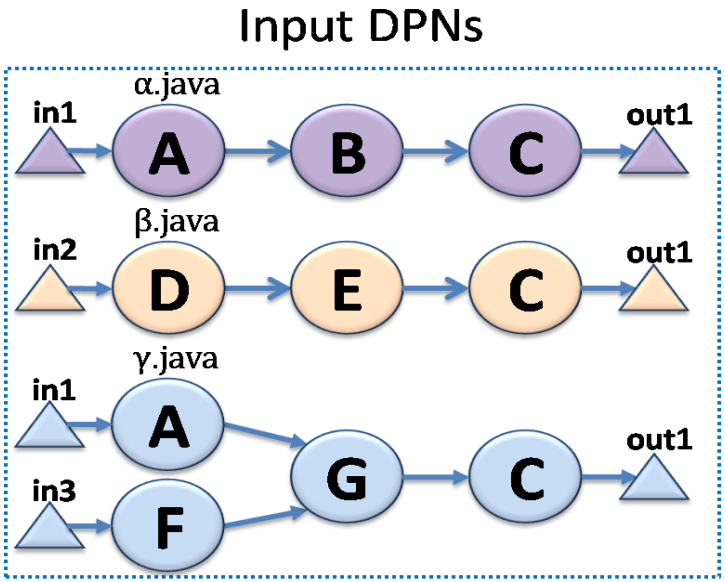
QUESTIONS



ACM International Conference on
Computing Frontiers 2015
May 18 – 21 2015, Ischia, Italy

Logic Regions Identification

Computational Actors

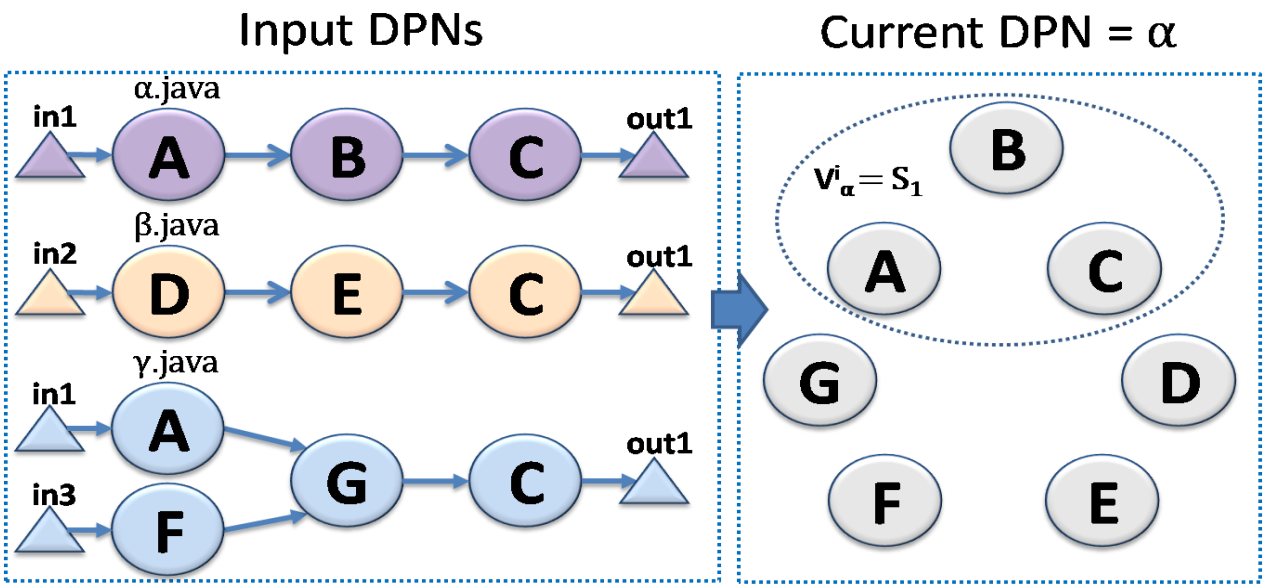


	α	β	γ
S_1			
S_2			
S_3			
S_4			
S_5			

EMPTY MAP

Logic Regions Identification

Computational Actors



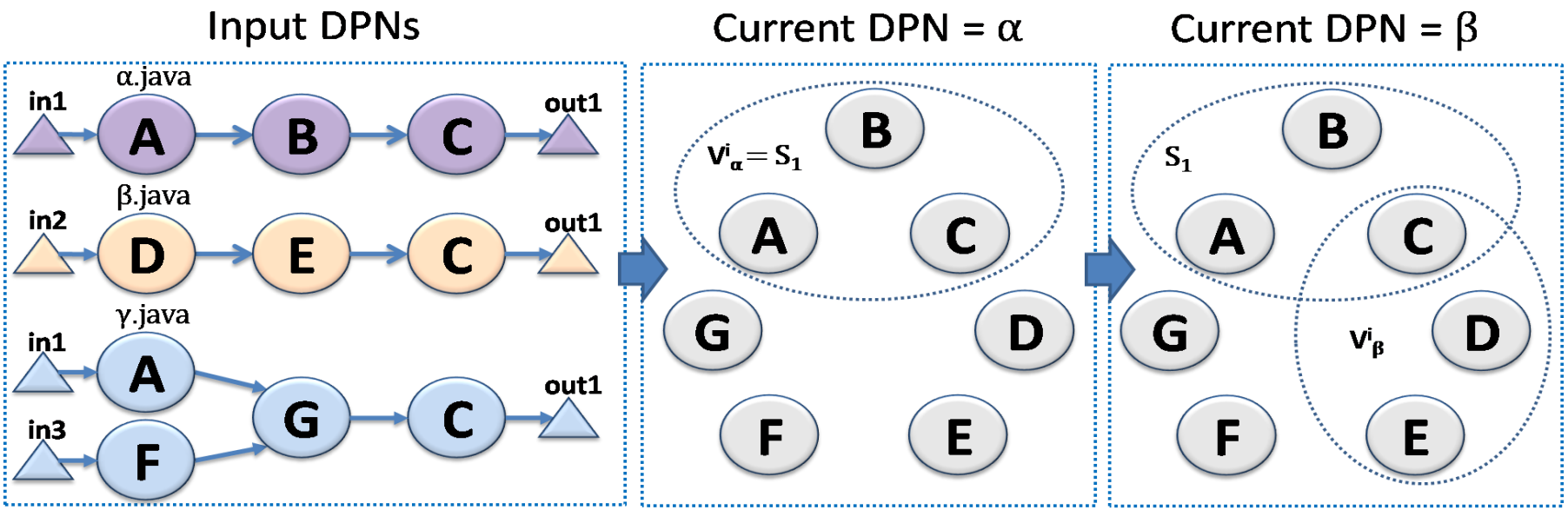
	α	β	γ
S_1			
S_2			
S_3			
S_4			
S_5			

EMPTY MAP

	α	β	γ
S_1	1	0	0
S_2			
S_3			
S_4			
S_5			

Logic Regions Identification

Computational Actors



	α	β	γ
S_1			
S_2			
S_3			
S_4			
S_5			

EMPTY MAP

	α	β	γ
S_1	1	0	0
S_2			
S_3			
S_4			
S_5			

	α	β	γ
S_1	1	0	0
S_2			
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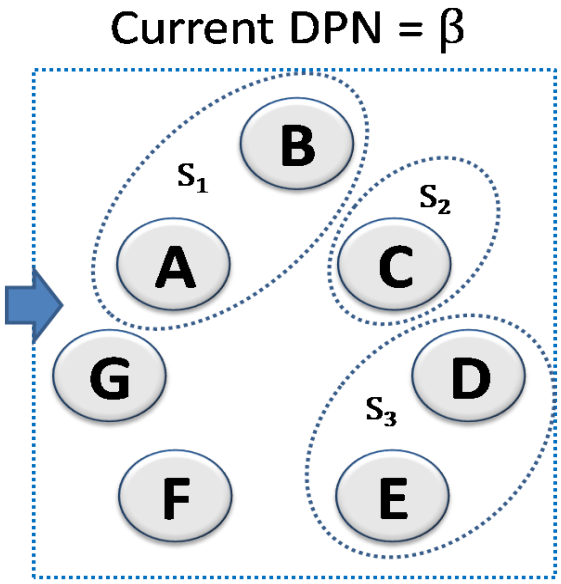
S_4			
S_5			

Logic Regions Identification

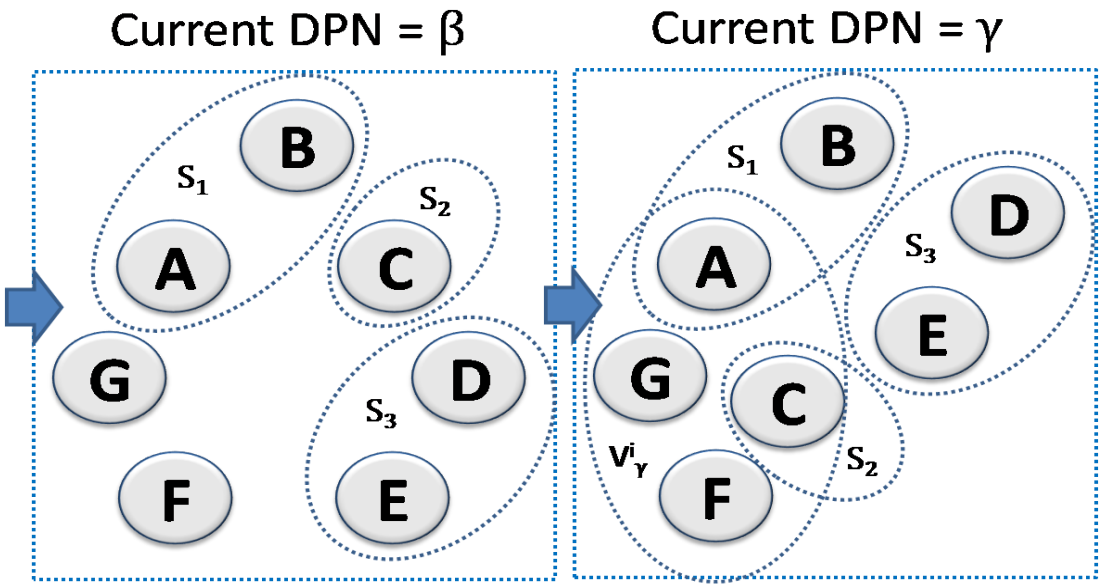
Computational Actors



	α	β	γ
S_1	1	0	0
S_2	1	1	0
S_3	0	1	0
S_4			
S_5			

Logic Regions Identification

Computational Actors

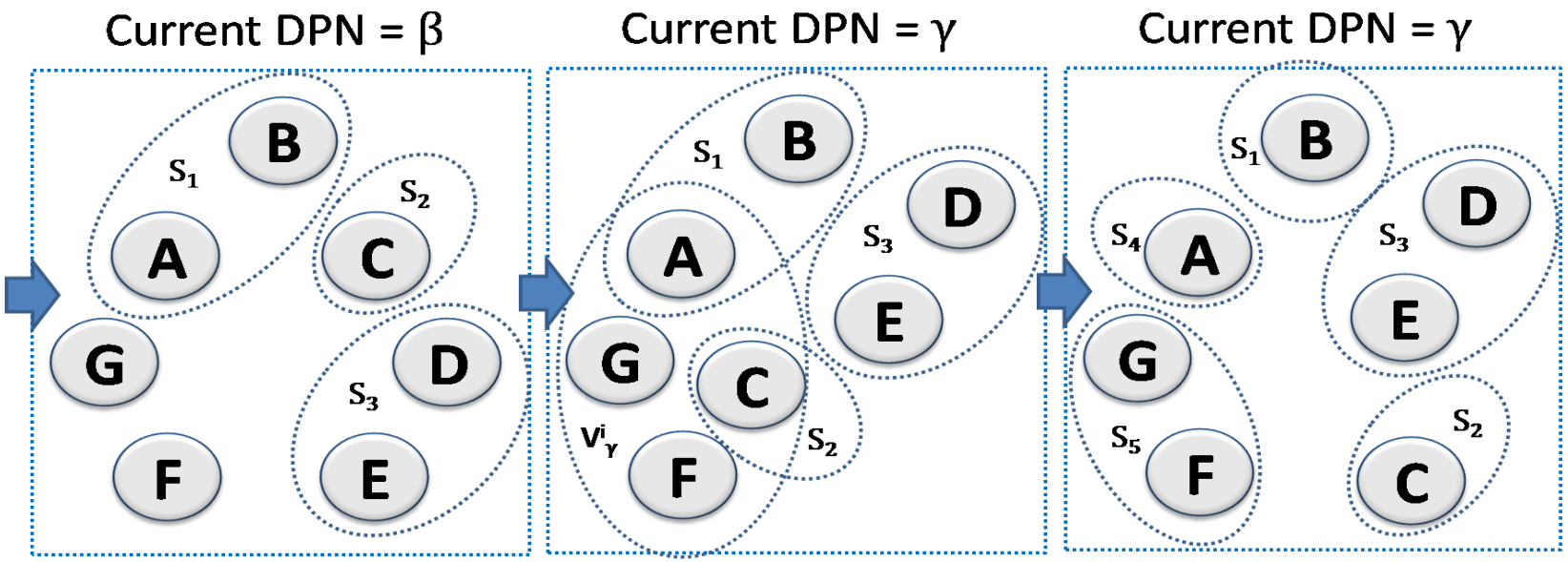


	α	β	γ
S_1	1	0	0
S_2	1	1	0
S_3	0	1	0
S_4			
S_5			

	α	β	γ
S_1	1	0	0
S_2	1	1	0
S_3	0	1	0
S_4			
S_5			

Logic Regions Identification

Computational Actors



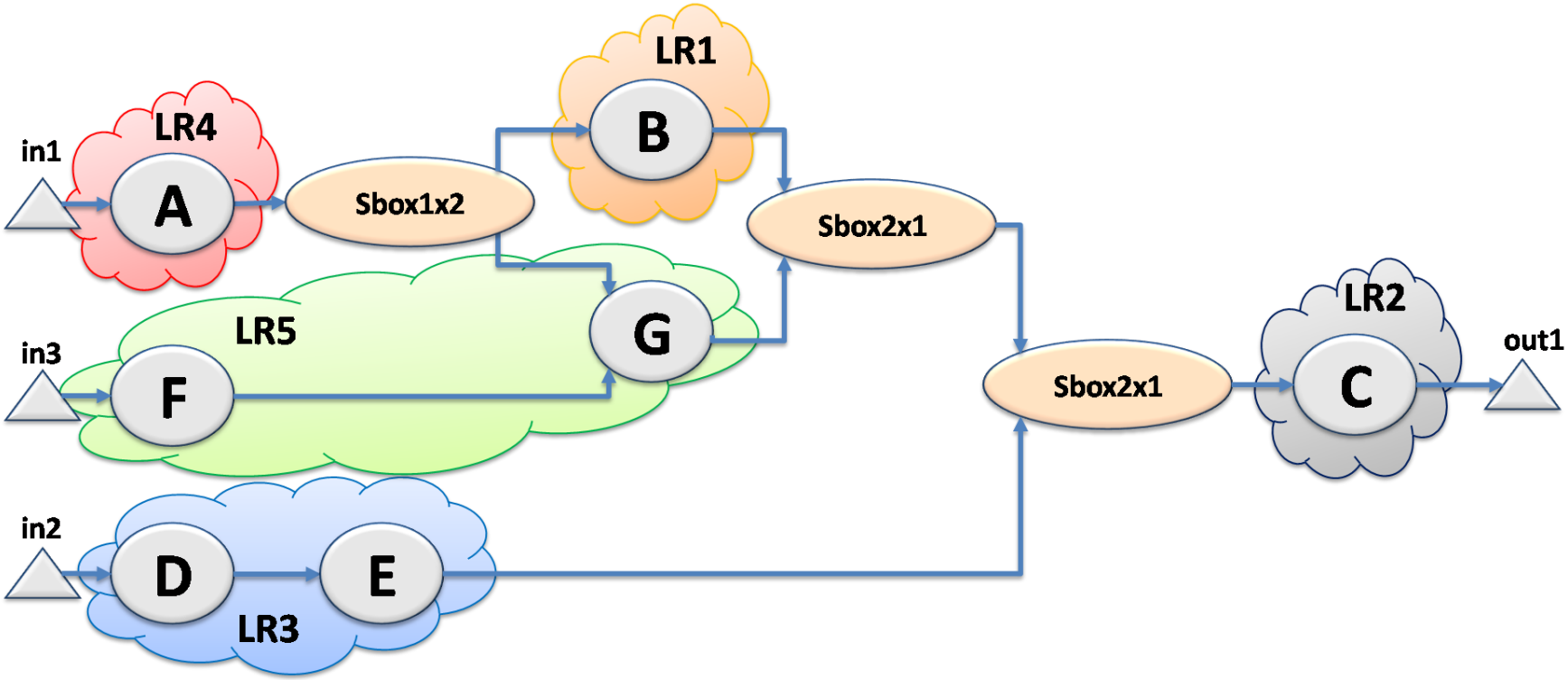
	α	β	γ
S_1	1	0	0
S_2	1	1	0
S_3	0	1	0
S_4			
S_5			

	α	β	γ
S_1	1	0	0
S_2	1	1	0
S_3	0	1	0
S_4			
S_5			

	α	β	γ
S_1	1	0	0
S_2	1	1	1
S_3	0	1	0
S_4	1	0	1
S_5	0	0	1

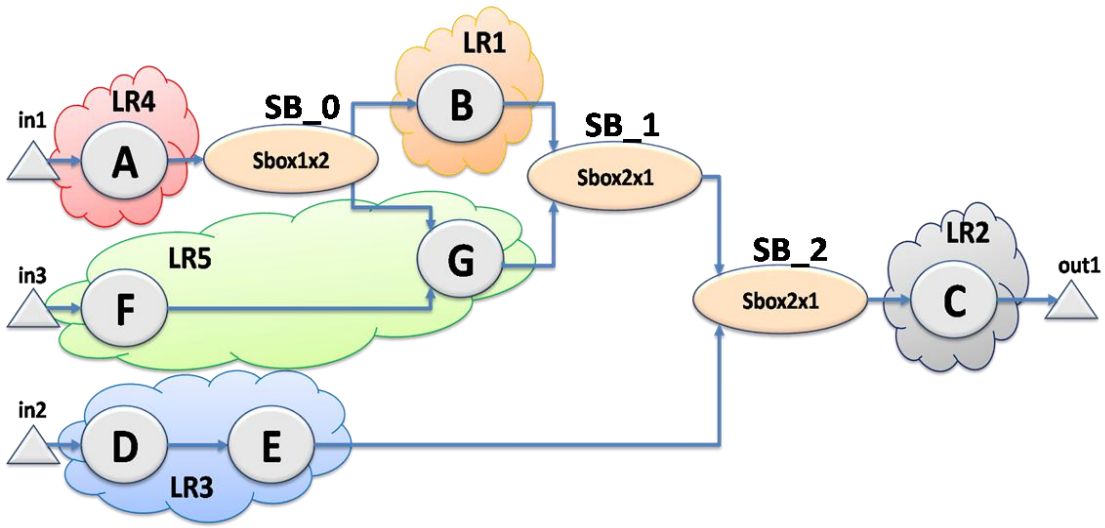
Logic Regions Identification

Computational Actors



Logic Regions Identification

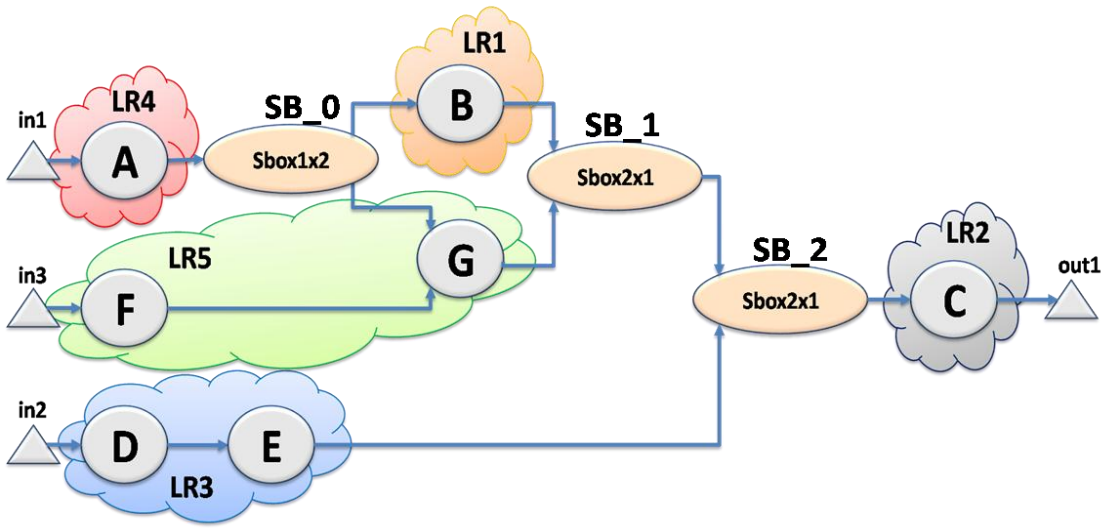
Sboxes



LR_MAP			
	α	β	γ
LR1	1	0	0
LR2	1	1	1
LR3	0	1	0
LR4	1	0	1
LR5	0	0	1

Logic Regions Identification

Sboxes

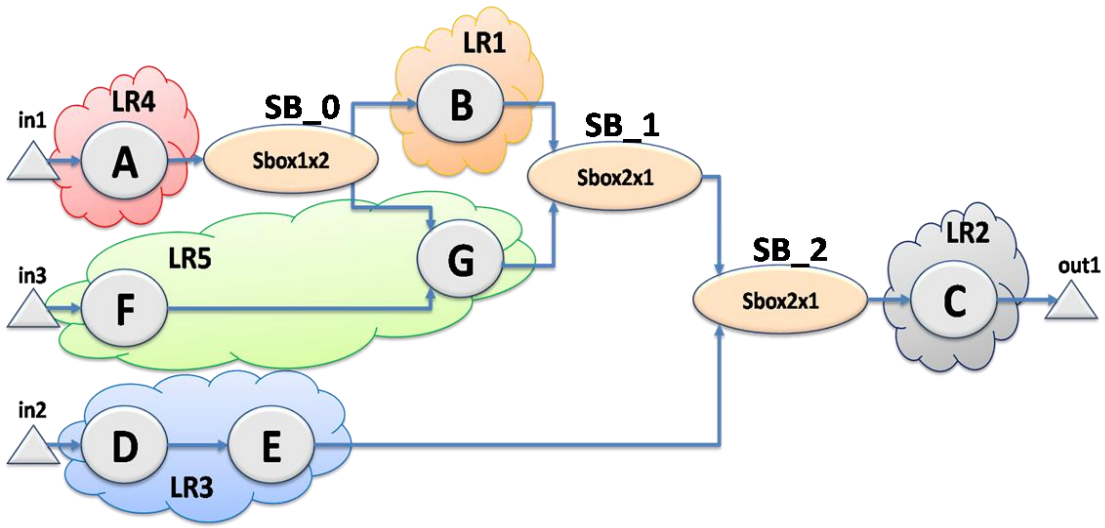


LR_MAP			
	α	β	γ
LR1	1	0	0
LR2	1	1	1
LR3	0	1	0
LR4	1	0	1
LR5	0	0	1

C_MAP			
	α	β	γ
SB_0	0	don't care	1
SB_1	0	dont'care	1
SB_2	0	1	0

Logic Regions Identification

Sboxes



LR_MAP			
	α	β	γ
LR1	1	0	0
LR2	1	1	1
LR3	0	1	0
LR4	1	0	1
LR5	0	0	1

C_MAP			
	α	β	γ
SB_0	0	don't care	1
SB_1	0	dont'care	1
SB_2	0	1	0

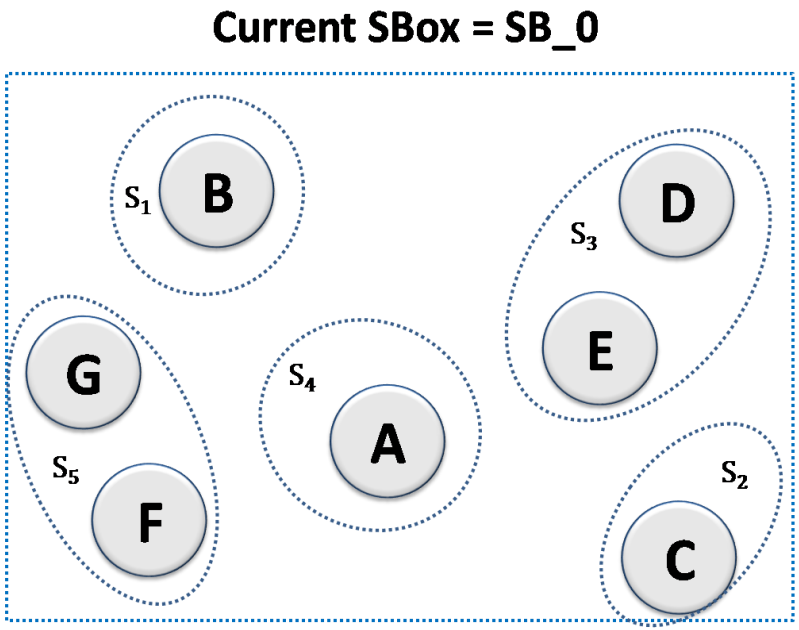
SB_MAP			
	α	β	γ
SB_0	1	0	1
SB_1	1	0	1
SB_2	1	1	1

Logic Regions Identification

Sboxes

Logic Regions Identification

Sboxes



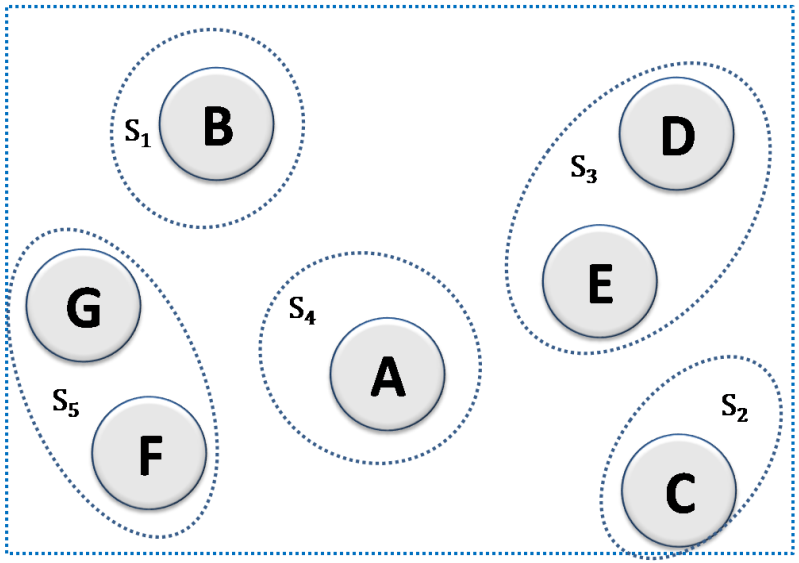
LR_MAP			
	α	β	γ
S_1	1	0	0
S_2	1	1	1
S_3	0	1	0
S_4	1	0	1
S_5	0	0	1

SB_MAP			
	α	β	γ
SB_0	1	0	1
SB_1	1	0	1
SB_2	1	1	1

Logic Regions Identification

Sboxes

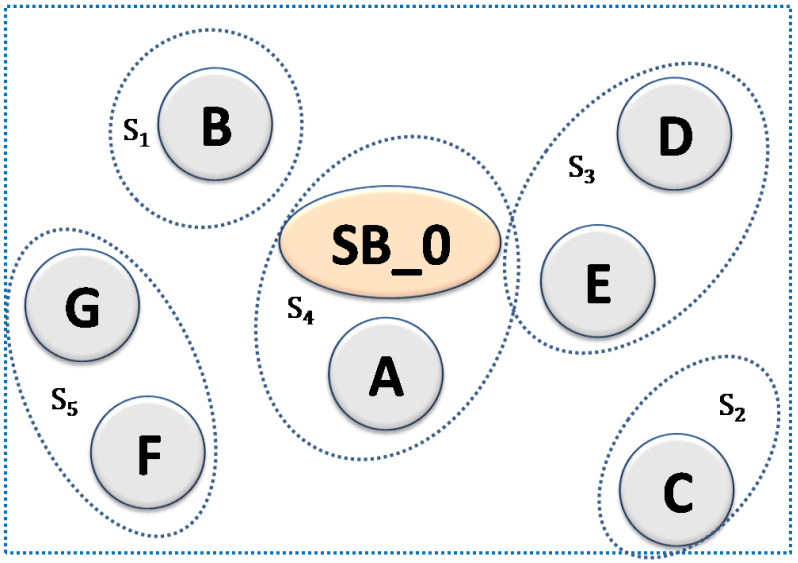
Current SBox = SB_0



LR_MAP	α	β	γ
S_1	1	0	0
S_2	1	1	1
S_3	0	1	0
S_4	1	0	1
S_5	0	0	1

SB_MAP	α	β	γ
SB_0	1	0	1
SB_1	1	0	1
SB_2	1	1	1

Current SBox = SB_0

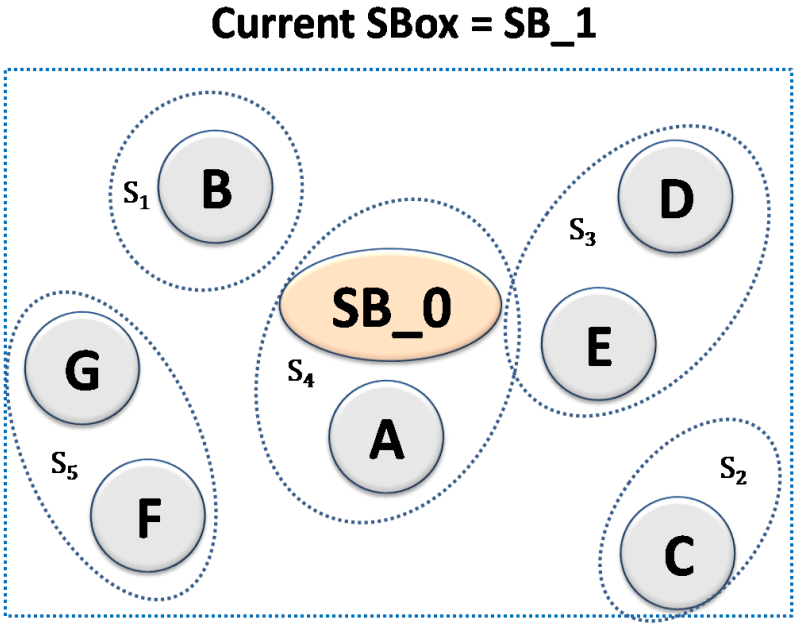


LR_MAP	α	β	γ
S_1	1	0	0
S_2	1	1	1
S_3	0	1	0
S_4	1	0	1
S_5	0	0	1

SB_MAP	α	β	γ
SB_0	1	0	1
SB_1	1	0	1
SB_2	1	1	1

Logic Regions Identification

Sboxes



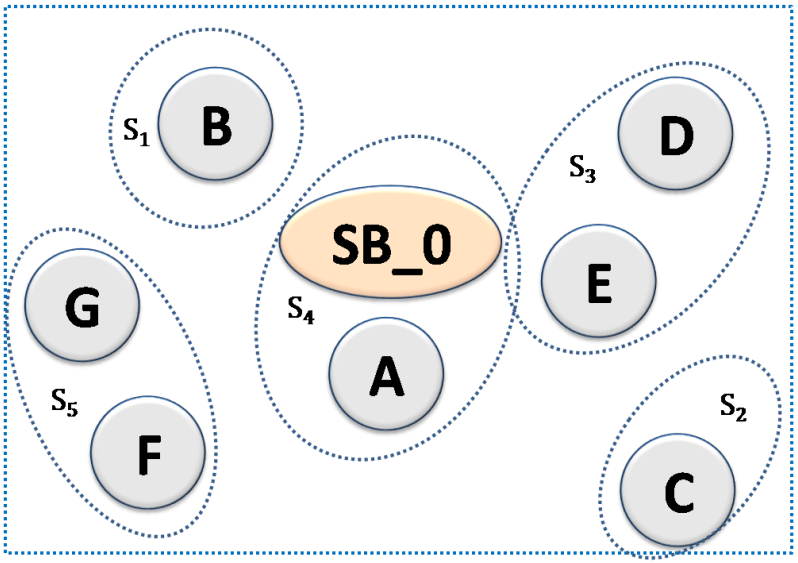
LR_MAP			
	α	β	γ
S_1	1	0	0
S_2	1	1	1
S_3	0	1	0
S_4	1	0	1
S_5	0	0	1

SB_MAP			
	α	β	γ
SB_0	1	0	1
SB_1	1	0	1
SB_2	1	1	1

Logic Regions Identification

Sboxes

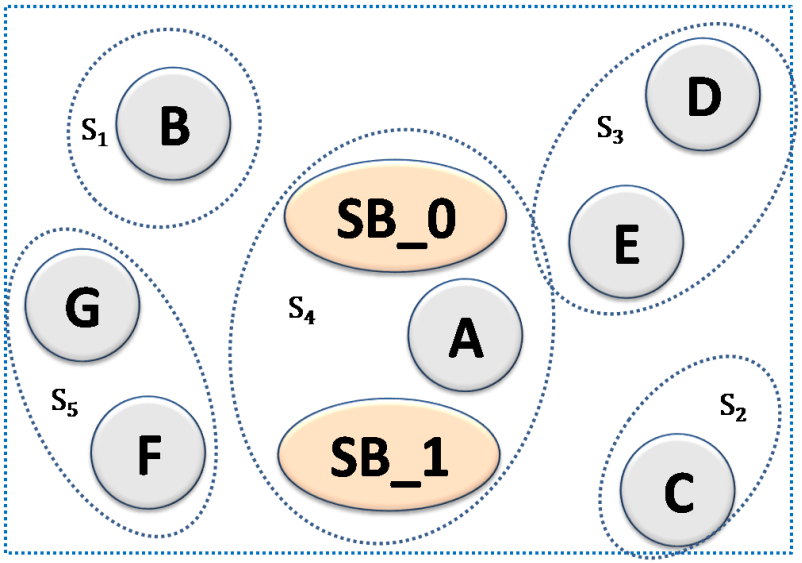
Current SBox = SB_1



LR_MAP			
	α	β	γ
S_1	1	0	0
S_2	1	1	1
S_3	0	1	0
S_4	1	0	1
S_5	0	0	1

SB_MAP			
	α	β	γ
SB_0	1	0	1
SB_1	1	0	1
SB_2	1	1	1

Current SBox = SB_1

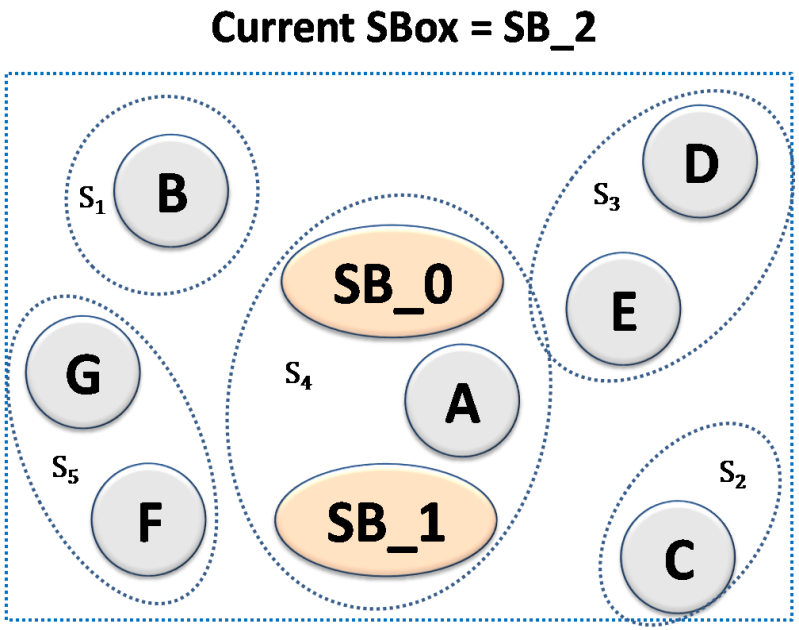


LR_MAP			
	α	β	γ
S_1	1	0	0
S_2	1	1	1
S_3	0	1	0
S_4	1	0	1
S_5	0	0	1

SB_MAP			
	α	β	γ
SB_0	1	0	1
SB_1	1	0	1
SB_2	1	1	1

Logic Regions Identification

Sboxes



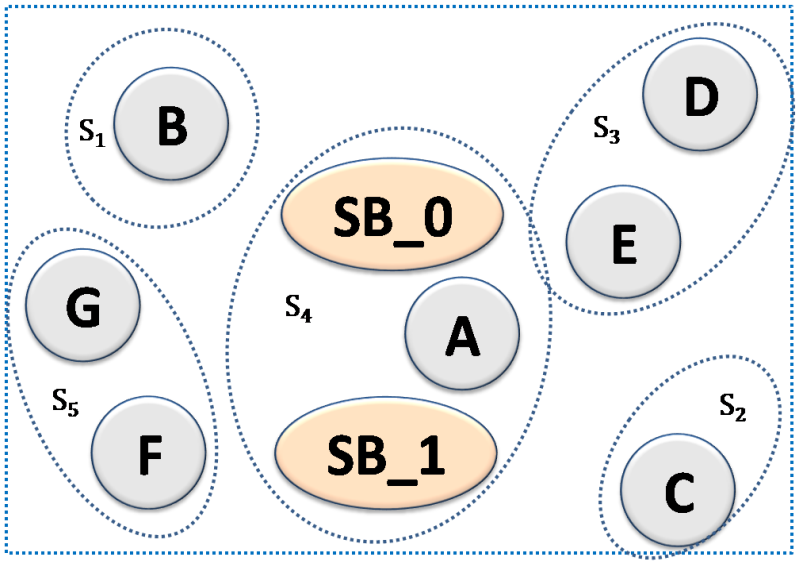
LR_MAP			
	α	β	γ
S_1	1	0	0
S_2	1	1	1
S_3	0	1	0
S_4	1	0	1
S_5	0	0	1

SB_MAP			
	α	β	γ
SB_0	1	0	1
SB_1	1	0	1
SB_2	1	1	1

Logic Regions Identification

Sboxes

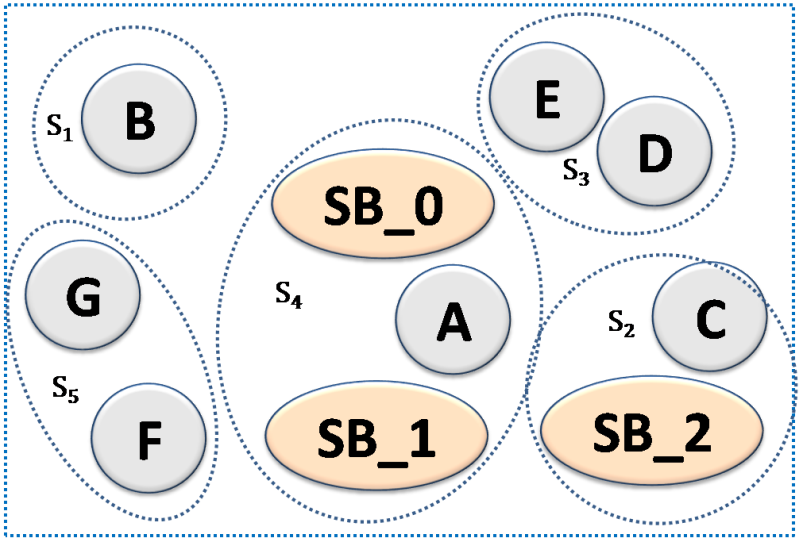
Current SBox = SB_2



LR_MAP			
	α	β	γ
S_1	1	0	0
S_2	1	1	1
S_3	0	1	0
S_4	1	0	1
S_5	0	0	1

SB_MAP			
	α	β	γ
SB_0	1	0	1
SB_1	1	0	1
SB_2	1	1	1

Current SBox = SB_2



LR_MAP			
	α	β	γ
S_1	1	0	0
S_2	1	1	1
S_3	0	1	0
S_4	1	0	1
S_5	0	0	1

SB_MAP			
	α	β	γ
SB_0	1	0	1
SB_1	1	0	1
SB_2	1	1	1

Logic Regions Identification

Sboxes