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Processing in Digital Media Technologies



**September 4th-6th, 2013,
Trieste, Italy**



Design Space Exploration and Profiling of Multi-Context Coarse-Grained Reconfigurable Systems

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University of Cagliari - ITALY





Outline

- Introduction
 - Background
 - Research Evolution
 - MDC Approach
 - Problem Definition
- The MDC DSE and profiler
 - Combinations Generator
 - Low-level Feedback Analysis
- Experimental Results
 - Design Under Test
 - Pareto Analysis
- Final Remarks



Background

- Systems and applications on the market are becoming every day more complex and power hungry.

ICT TRENDS

- Ubiquitous access
- Personalized services
- Delocalized computing and storage
- Massive data processing systems
- High-quality virtual reality
- Intelligent sensing
- High-performance real-time embedded computing

EXAMPLES

- Domestic robot
- Telepresence
- The car of the future
- Aerospace and avionics
- Human ++
- Computational science
- Realistic games
- Smart camera networks

SOURCE: <http://www.hipeac.net/roadmap>

- Flexibility, Portability, wearability, implantability, battery life limits, real-time along with computational correctness needs to be taken into account.



Background

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**INTEGRATION, SPECIALIZATION and HIGH PERFORMANCE
REQUIREMENTS**

in such

**COMPLEX COMPUTATIONAL HUNGRY ENVIRONMENTS
has threatened the
TRADITIONAL DESIGN FLOW.**

SOURCE: <http://www.hipeac.net/roadmap>

- Flexibility, Portability, wearability, implantability, battery life limits, real-time along with computational correctness needs to be taken into account.



Research Evolution

Reconfigurable Video Coding modularity coupled with hw reconfiguration has been exploited to efficiently map on an unique substrate multiple applications (Multi-Dataflow Composer tool).



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- High-level dataflow combination tool, front-end of the actual MDC tool. [DASIP 2010]
- Multi-Dataflow Composer (MDC) tool: concrete definition of the hardware template and of the D-MoC based mapping strategy. [DASIP 2011, JRTIP]





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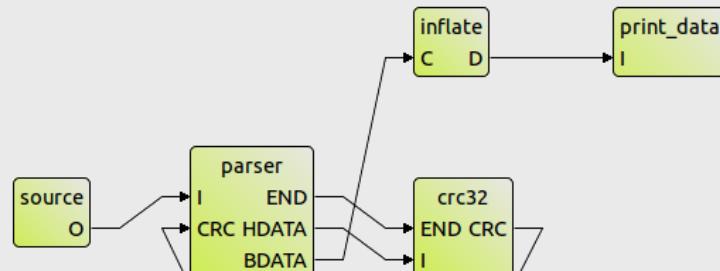
- High-level dataflow combination tool, front-end of the actual MDC tool. [DASIP 2010]
- Multi-Dataflow Composer (MDC) tool: concrete definition of the hardware template and of the D-MoC based mapping strategy. [DASIP 2011, JRTIP]
- Integration of the full high-level to hw composition and generation framework. [ISCAS 2012]





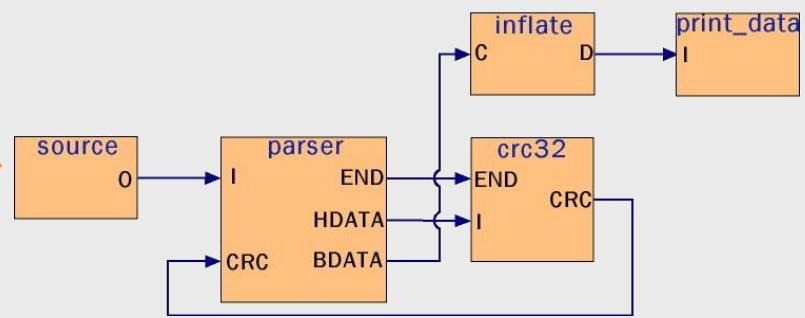
MDC Approach: basics

Modular Dataflow Formalism

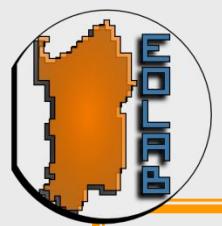


[SOURCE: <http://orcc.sourceforge.net/>]

HW Platform

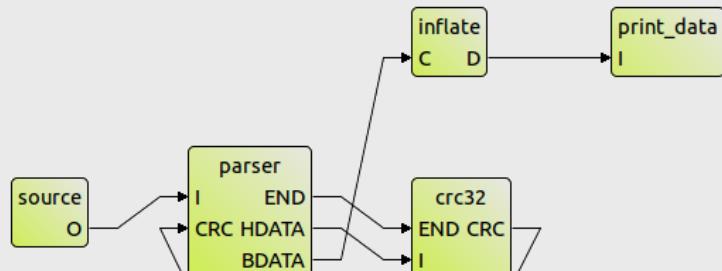


1:1



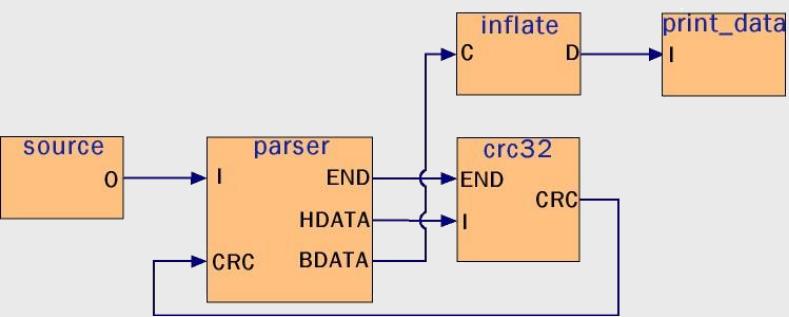
MDC Approach: basics

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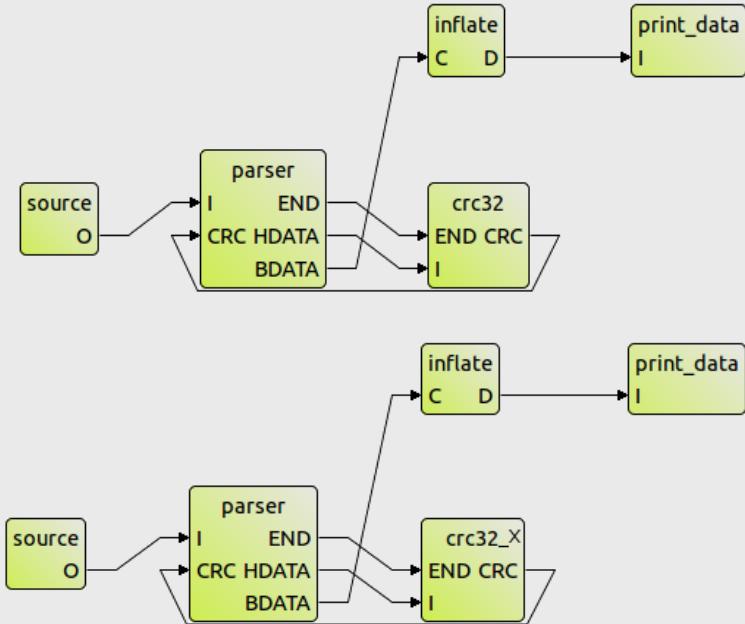


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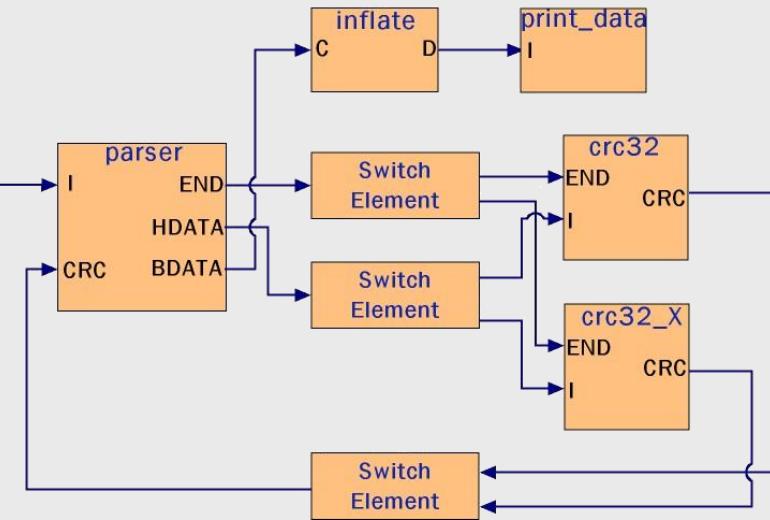
HW Platform



Modular Dataflow Formalism



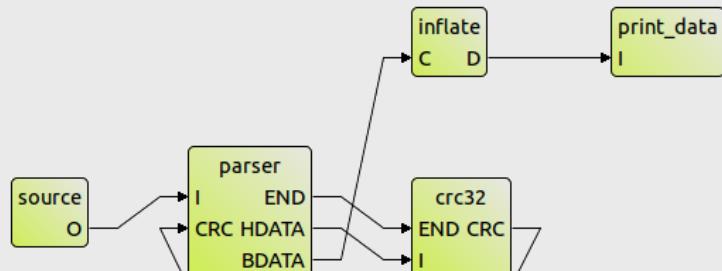
Coarse Grained Reconfigurable HW Platform





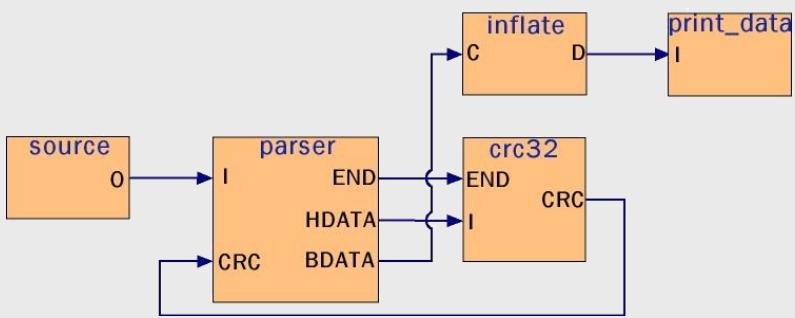
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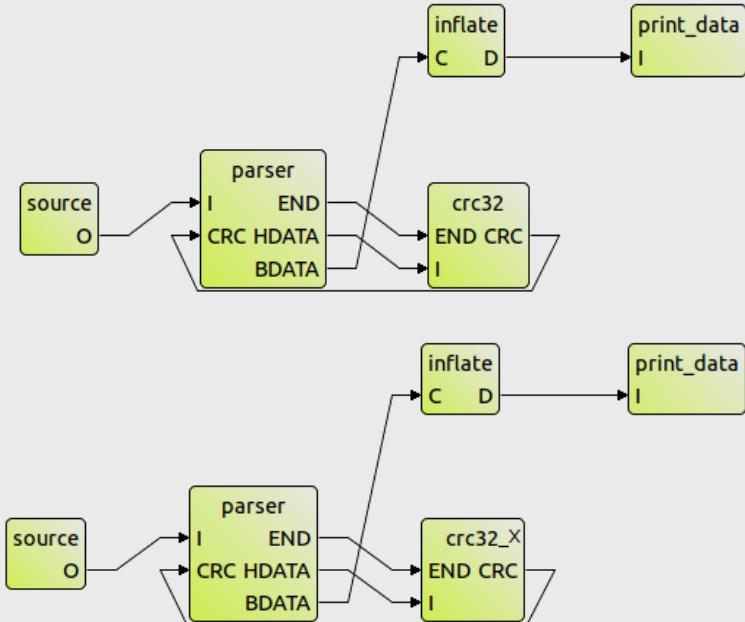


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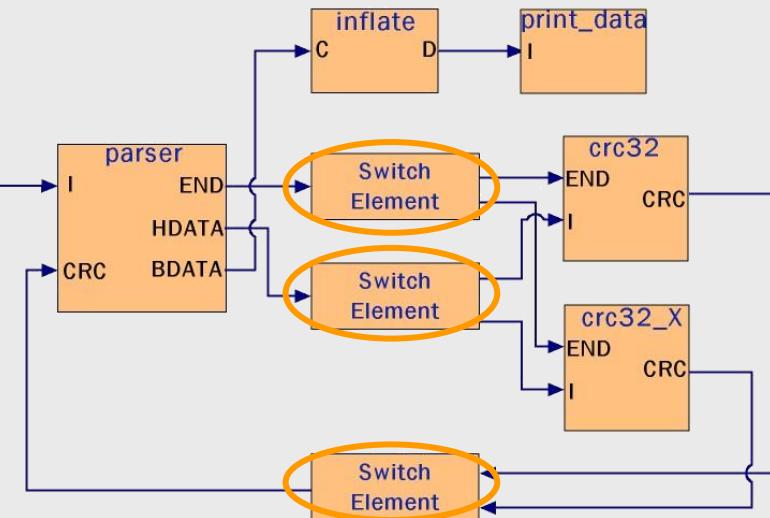
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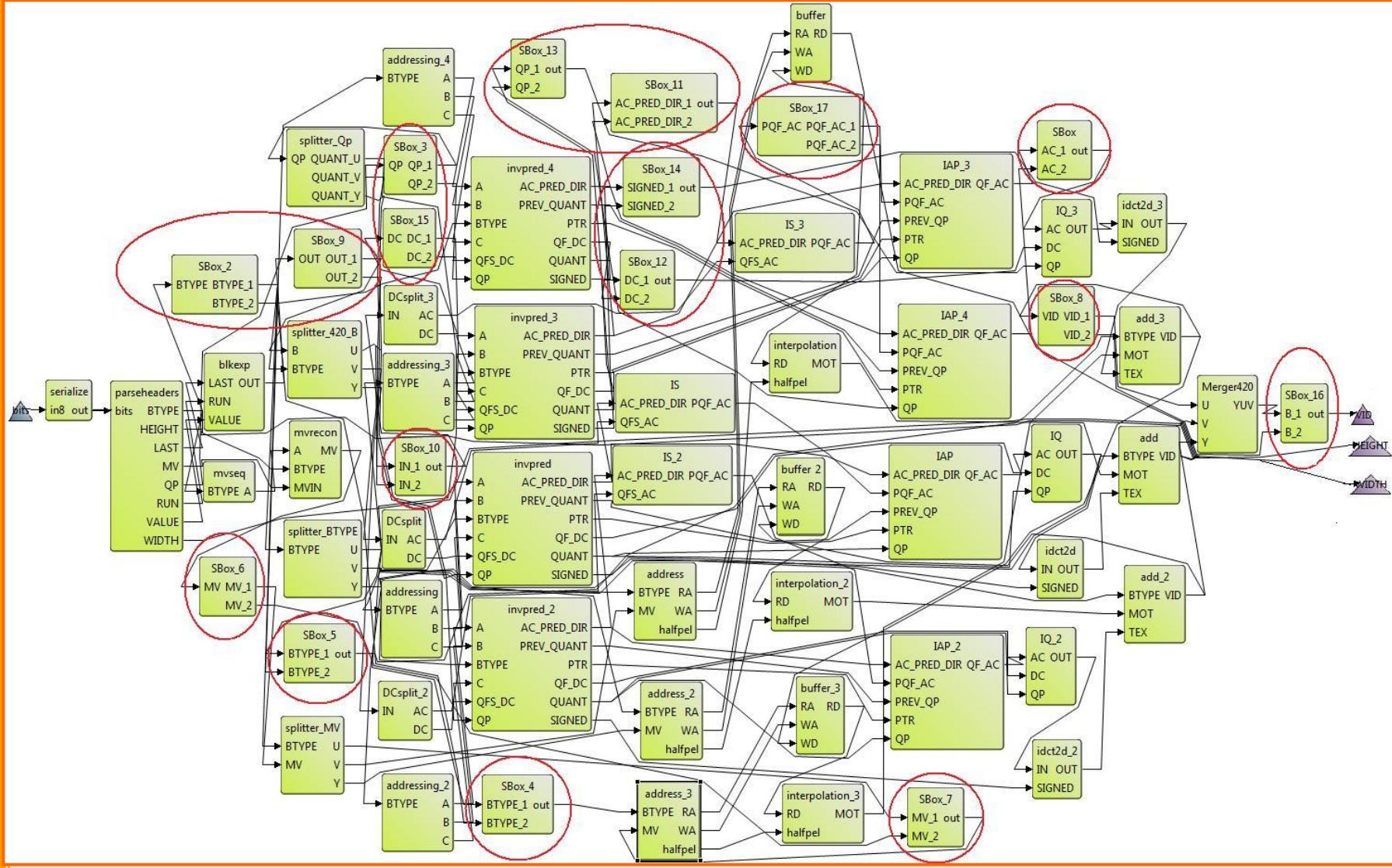


Coarse Grained Reconfigurable HW Platform



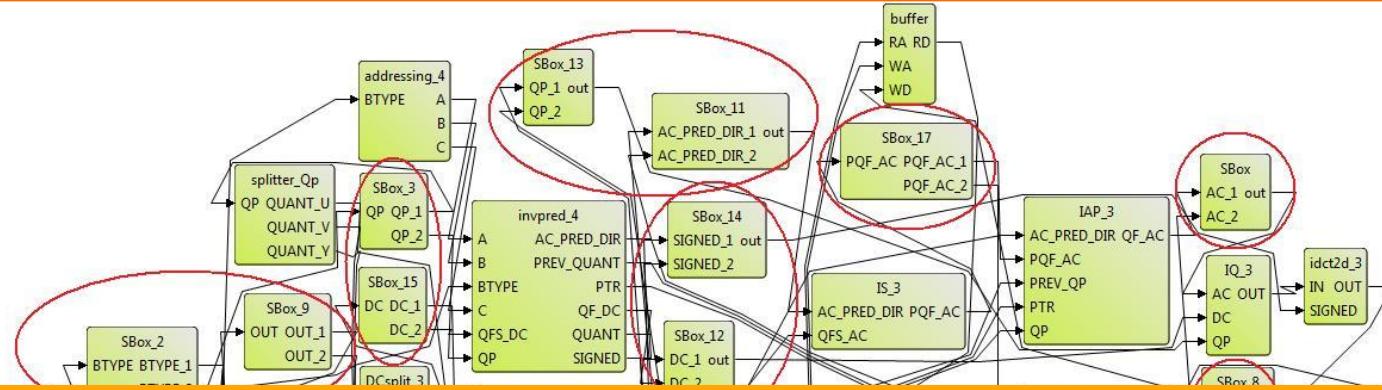


MDC Approach: complexity



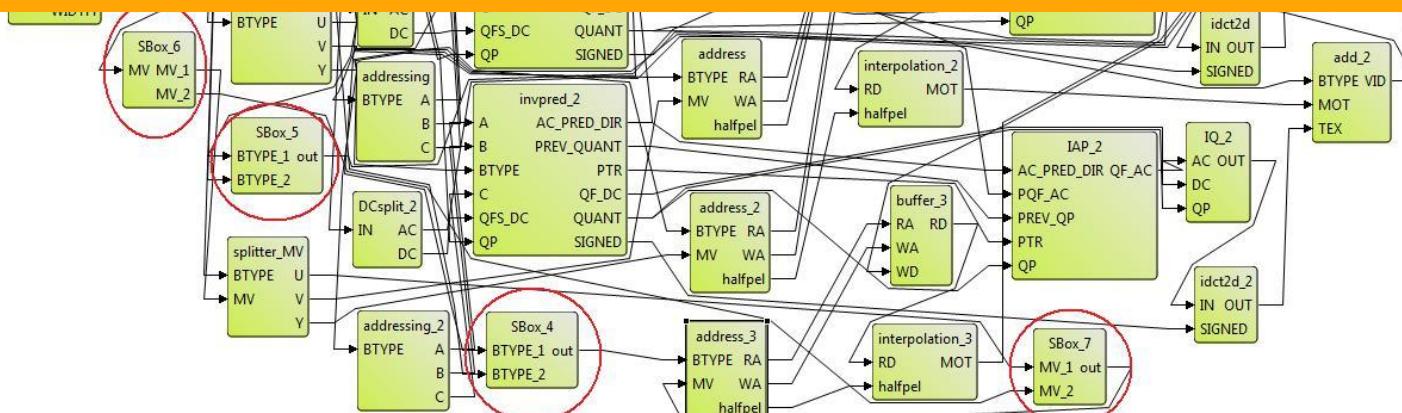


MDC Approach: complexity



COMPLEX, ERROR PRONE AND TIME CONSUMING:

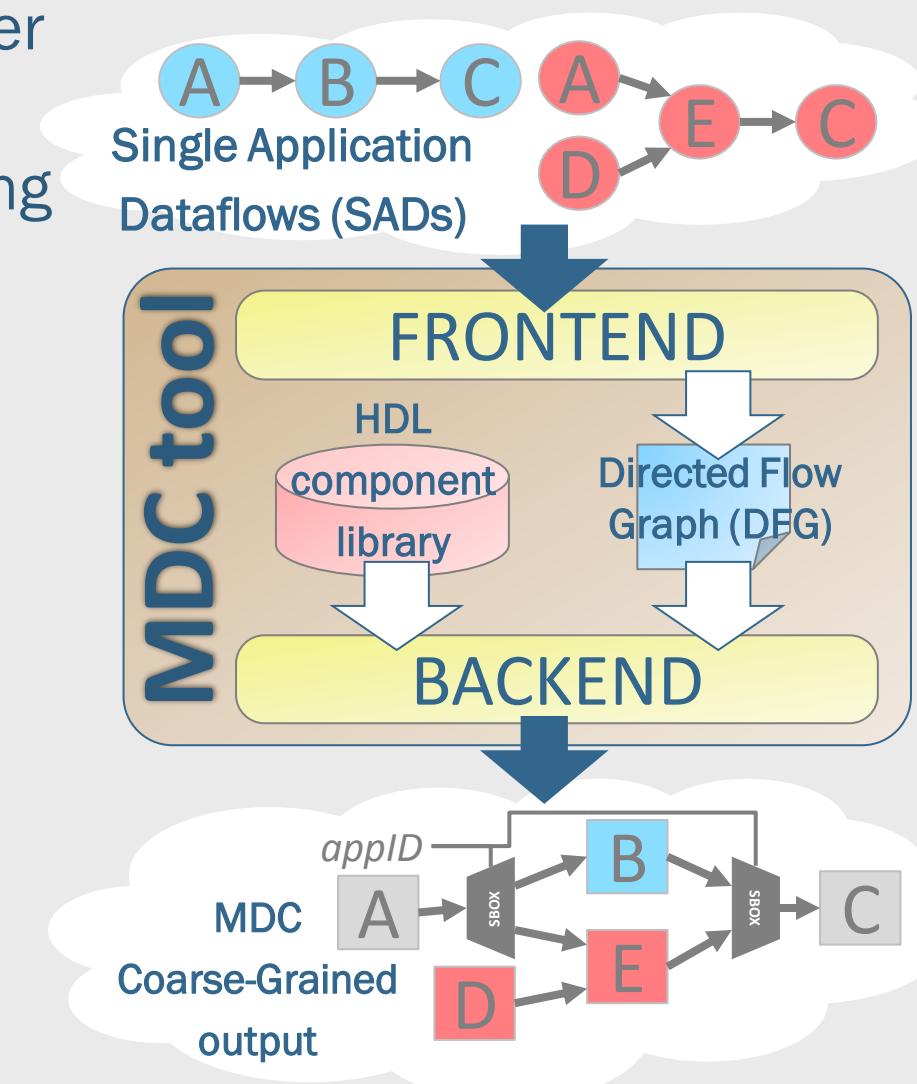
- PLATFORM COMPOSITION
- RECONFIGURATION MANAGEMENT





MDC Approach: the tool

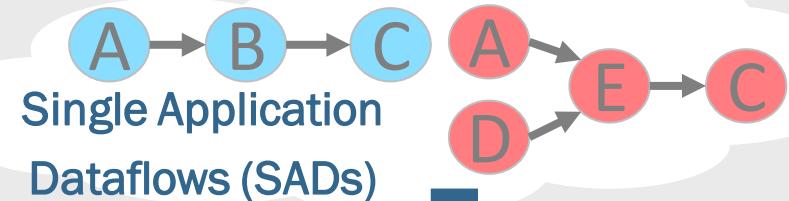
- The Multi-Dataflow Composer (MDC) tool **IS** an automatic platform generator combining different dataflow networks (SADs) on a coarse-grained reconfigurable template.
- The MDC **IS** responsible of providing runtime programmability of the hw substrate to switch among given the SADs.
- The MDC **IS NOT** capable of High Level Synthesis from SAD to hw.





MDC Approach: the tool

- The Multi-Dataflow Composer (MDC) tool **IS** an automatic platform generator combining



benefits of the MDC approach have been already demonstrated

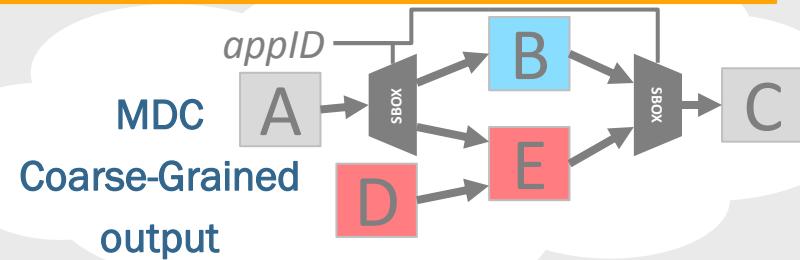
[F. Palumbo et.al., "The multi-dataflow composer tool: generation of on-the-fly reconfigurable platforms", in Jnl of Real Time Image Processing]

BUT

an early stage trade-off analysis may be extremely useful

given the SADs.

- The MDC **IS NOT** capable of High Level Synthesis from SAD to hw.



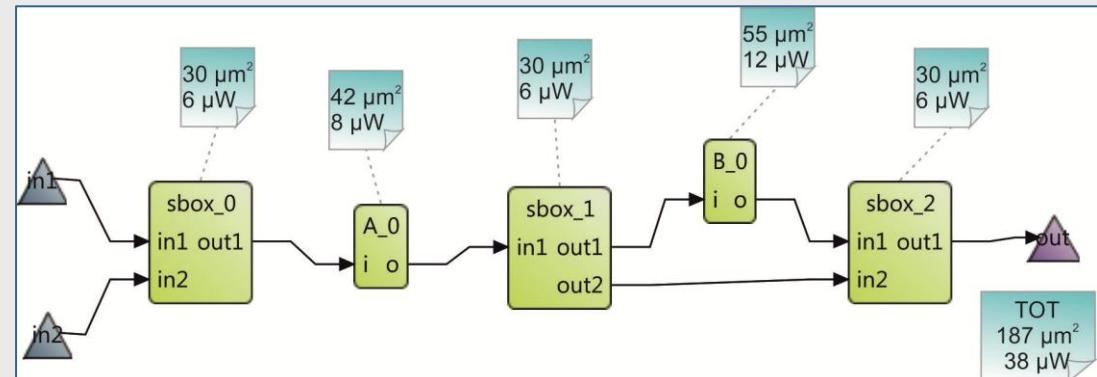
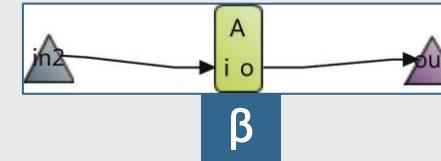
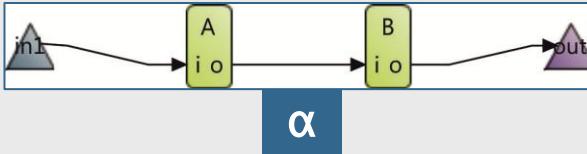


Problem Statement



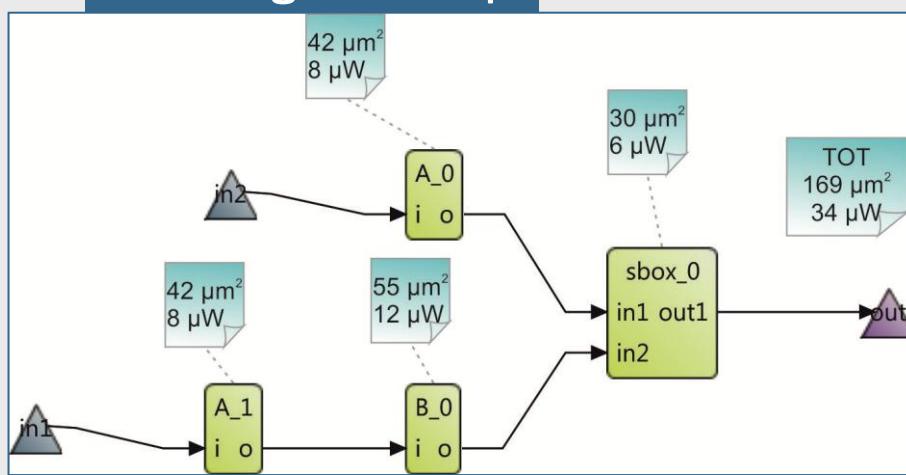
Problem Statement

- Merging all the SADs is **not always** the best choice



not merged α and β

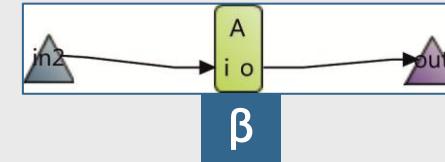
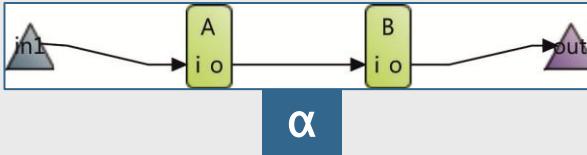
merged α and β



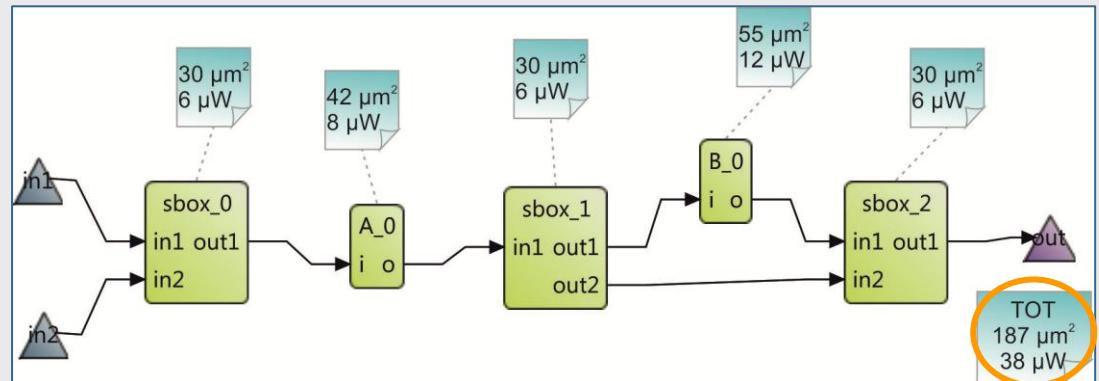


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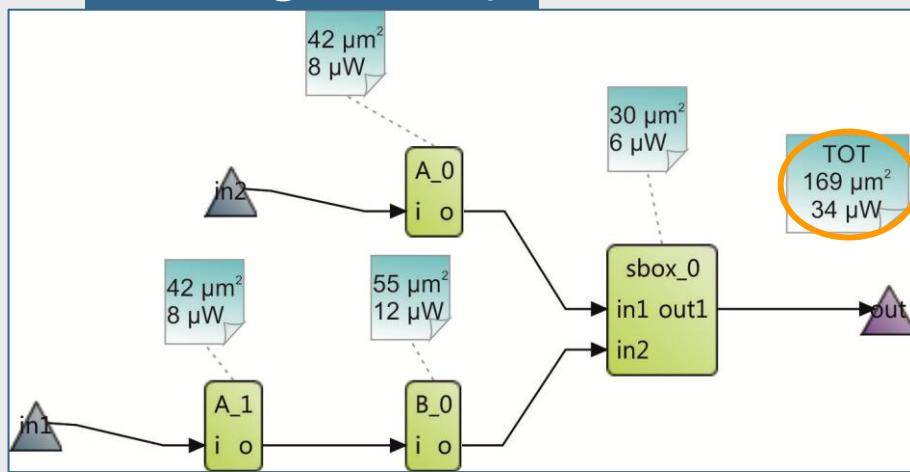
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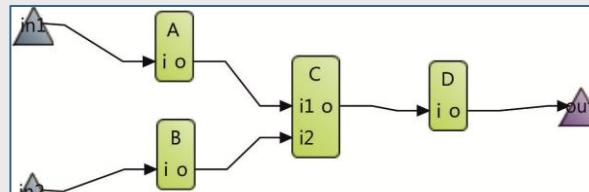
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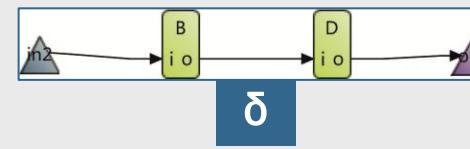


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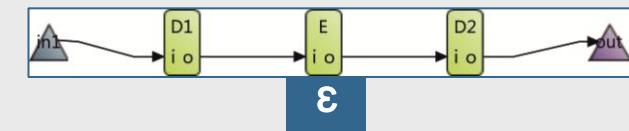
- Merging all the SADs is **not always** the best choice
- Different outputs with **different orders** of the SADs



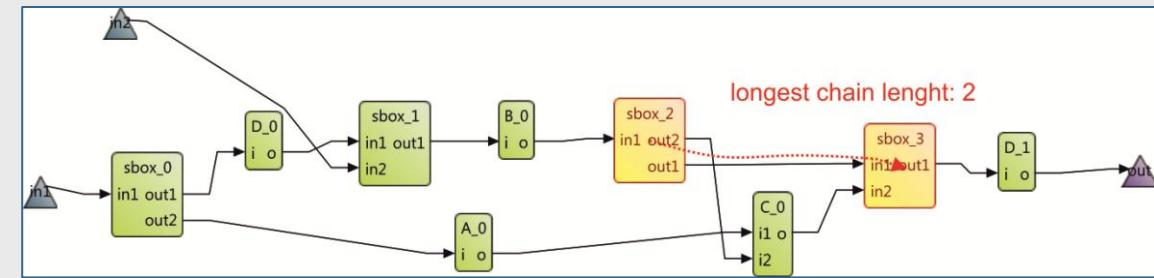
γ



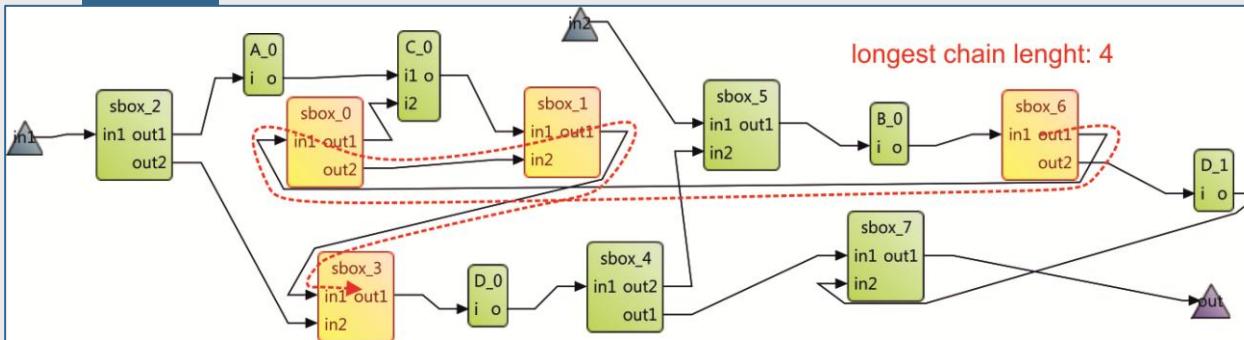
δ



ϵ



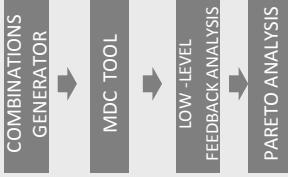
$\gamma\delta\epsilon$

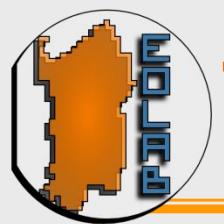


longest chain lenght: 4

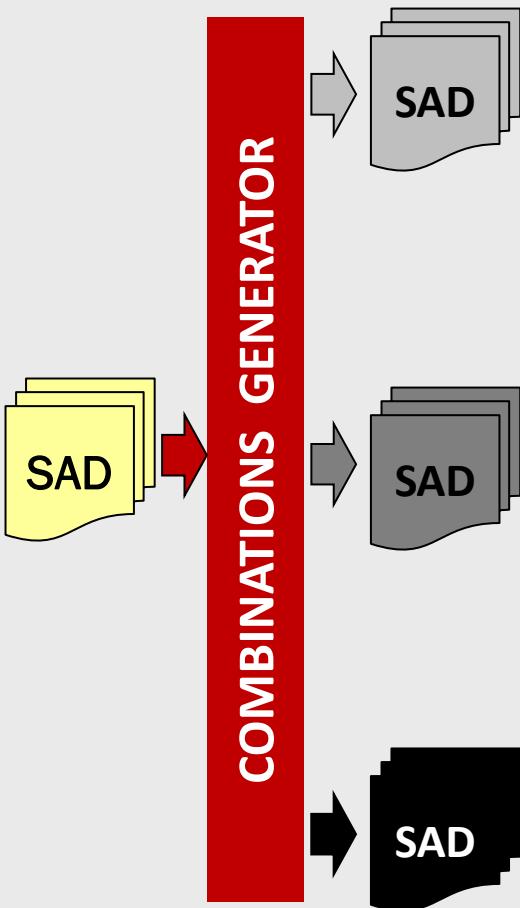
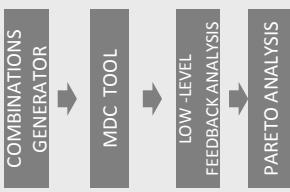


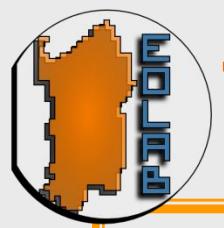
The MDC DSE and profiler



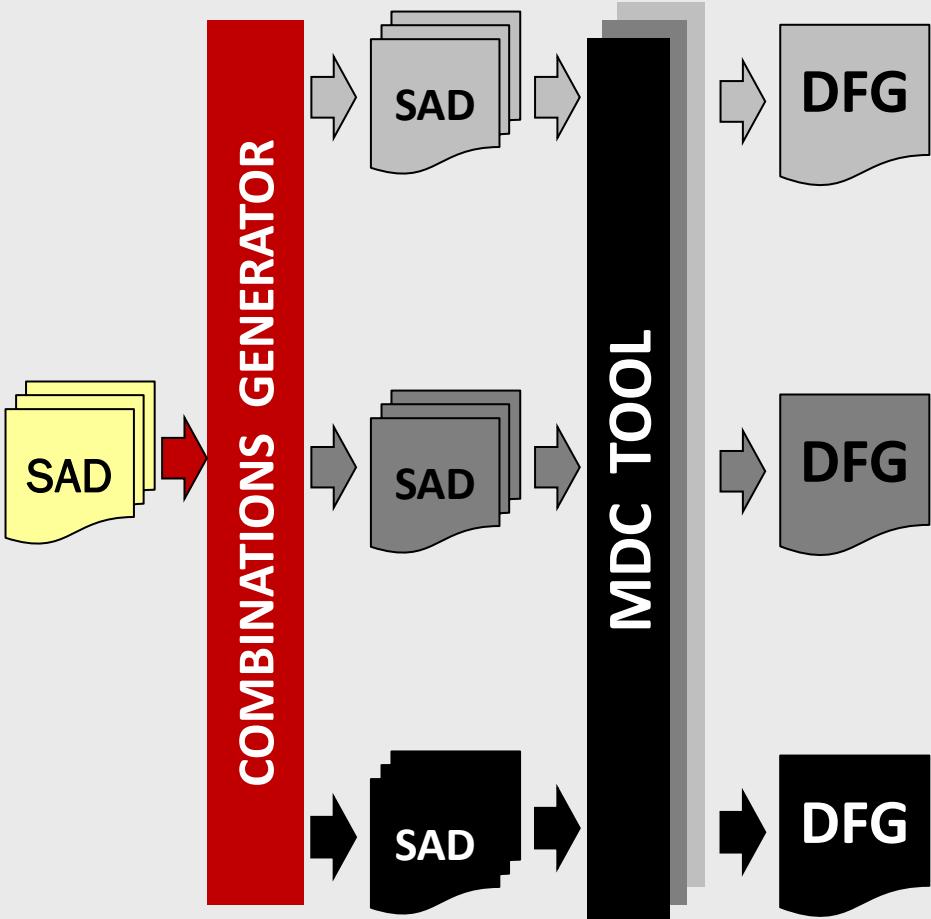
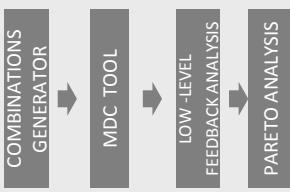


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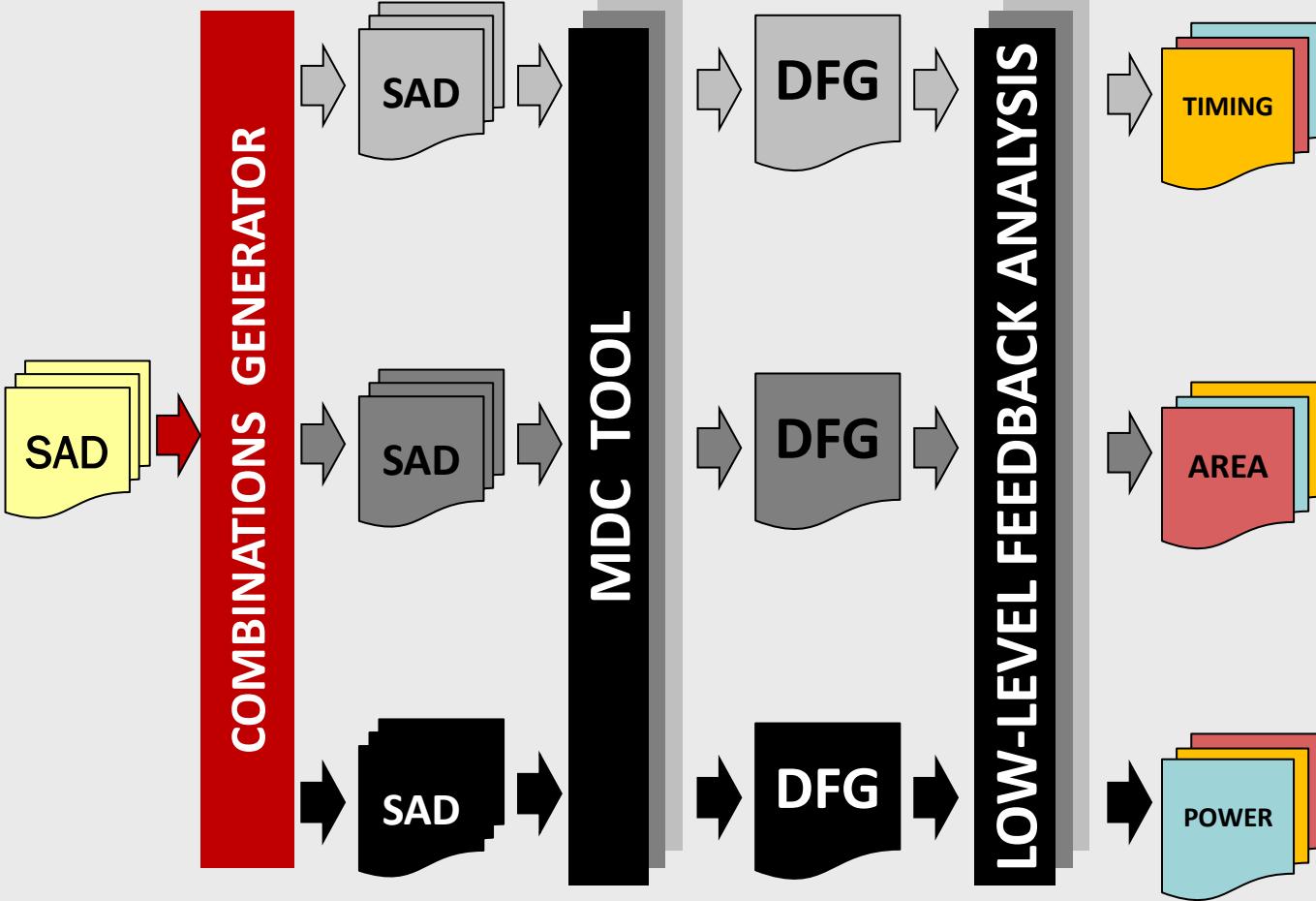
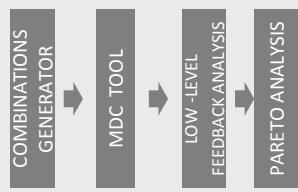


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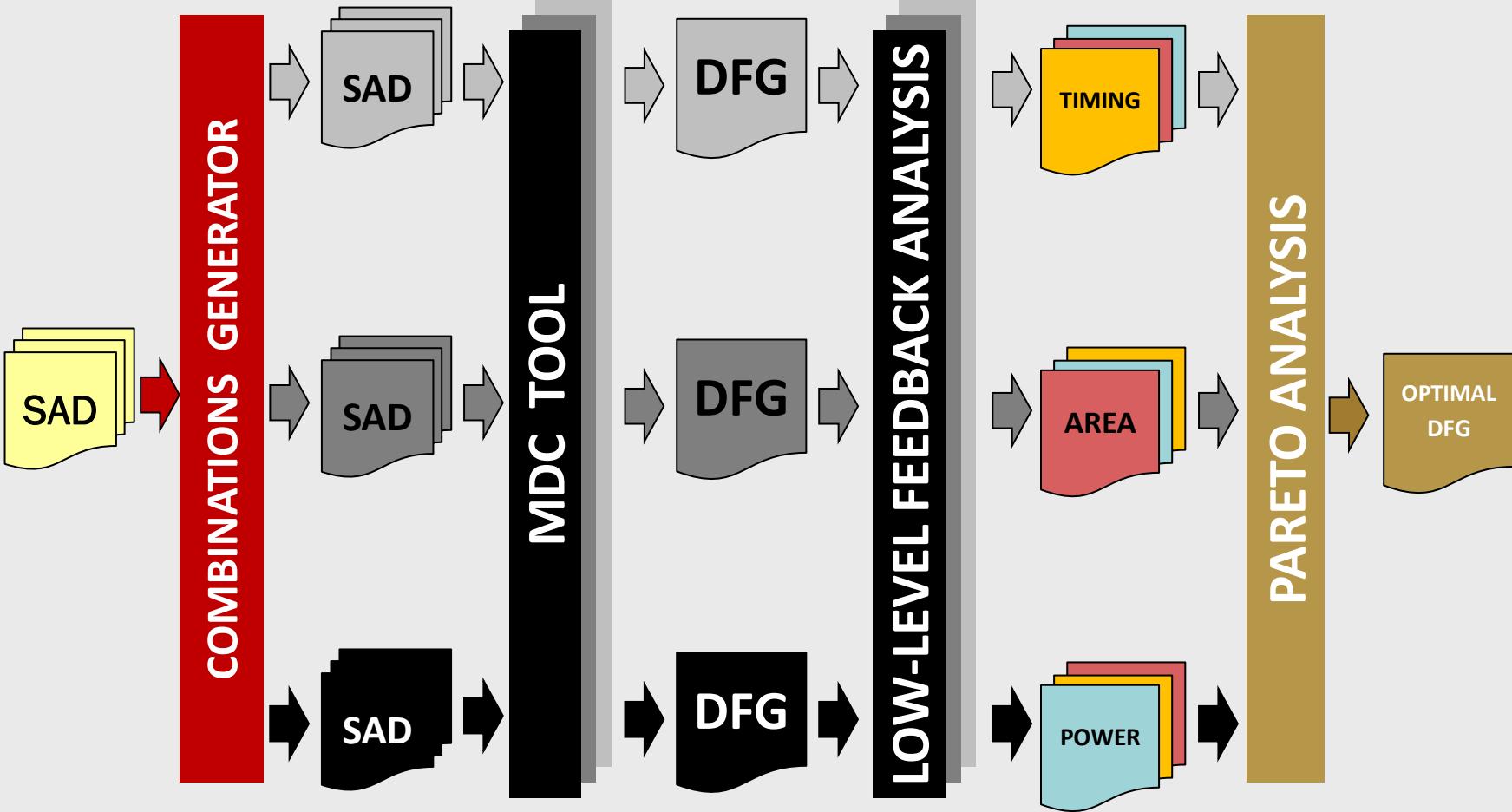
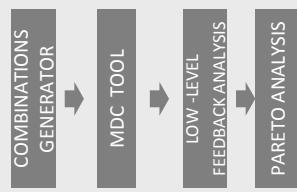


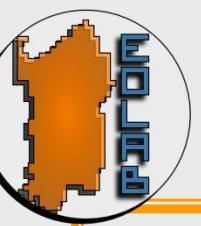
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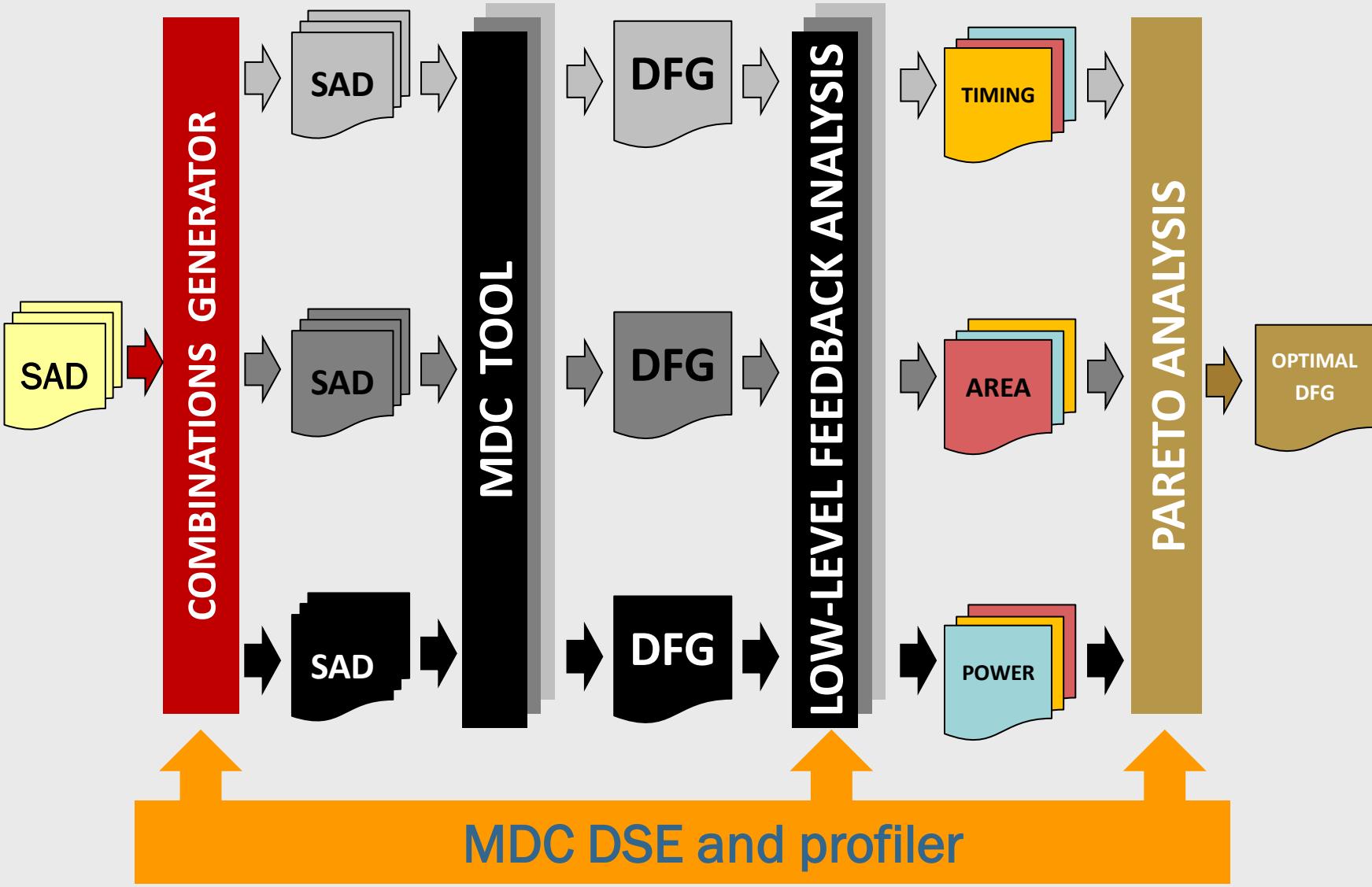
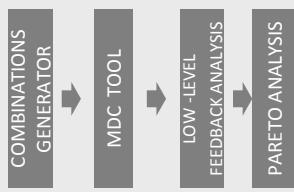
The MDC DSE and profiler





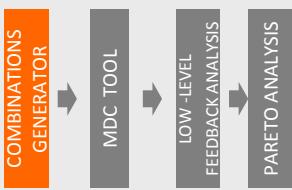
The MDC DSE and profiler

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Combinations Generator (1)



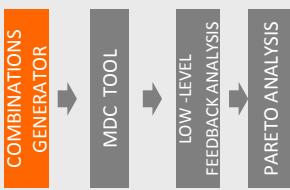
Number and type of combinations:

- ***D_notMer***: not merged composition of the N input SADs in placed in parallel;
- ***D_Mer***: as much resources as possible are shared merging together all the N input SADs;
- ***D_partMer***: it is not maximized resource sharing; any DFG is composed of i not merged SADs in parallel with one of the permutations f the other $N-i$.

$$D = D_{notMer} + D_{Mer} + D_{partMer} = 1 + N! + \sum_{K=2}^{N-1} \prod_{j=k}^N j$$



Combinations Generator (2)



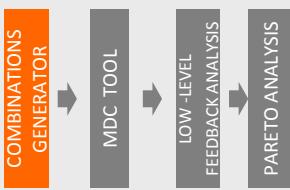
$$N = 4$$

$$SADs = \{D_1, D_2, D_3, D_4\}$$

$$D = D_{notMer} + D_{Mer} + D_{partMer} = 61$$



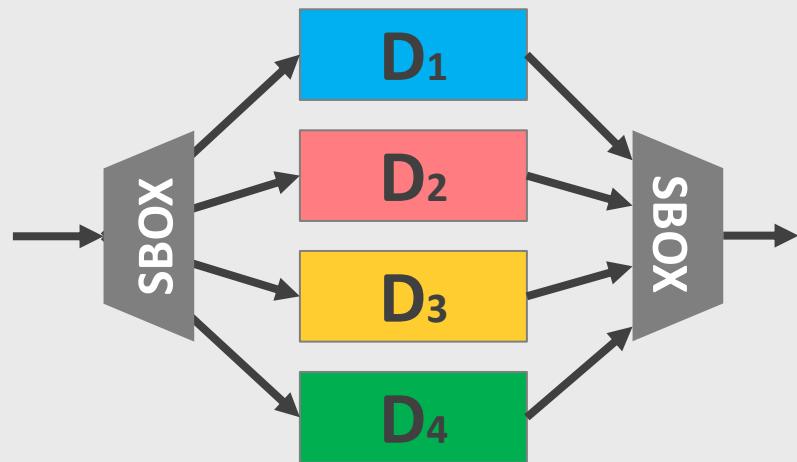
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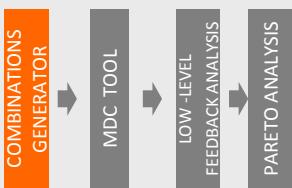
$$D = D_{notMer} + D_{Mer} + D_{partMer} = 61$$



$$D_{notMer} = 1$$



Combinations Generator (2)



$$N = 4$$

$$SADs = \{D_1, D_2, D_3, D_4\}$$

$$D = D_{notMer} + D_{Mer} + D_{partMer} = 61$$

$$D_{1234} = D_1 + D_2 + D_3 + D_4$$

$$D_{1243} = D_1 + D_2 + D_4 + D_3$$

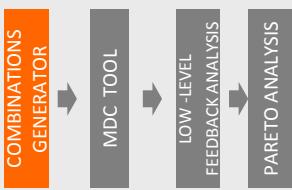
⋮

$$D_{4321} = D_4 + D_3 + D_2 + D_1$$

$$D_{Mer} = N! = 1 \cdot 2 \cdot 3 \cdot 4 = 24$$



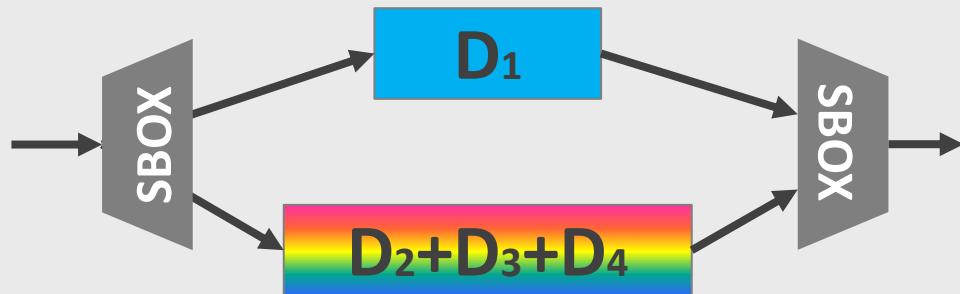
Combinations Generator (2)



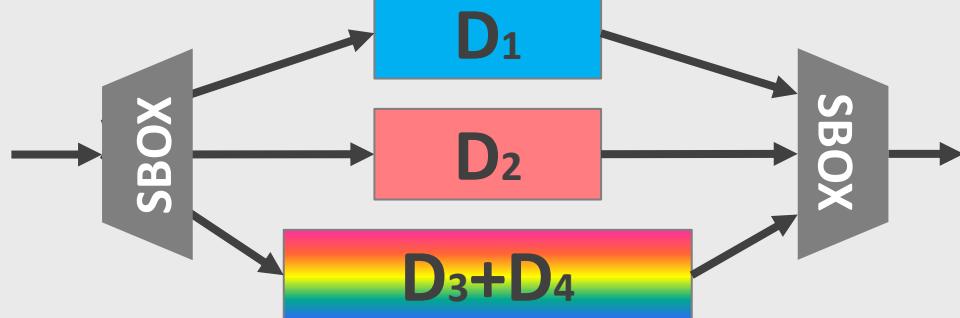
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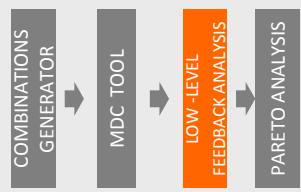


$$D_{partMer} = \sum_{K=2}^3 \prod_{j=k}^4 j = (2 \cdot 3 \cdot 4) + (3 \cdot 4) = 36$$





Low-level Feedback Analysis: area and power



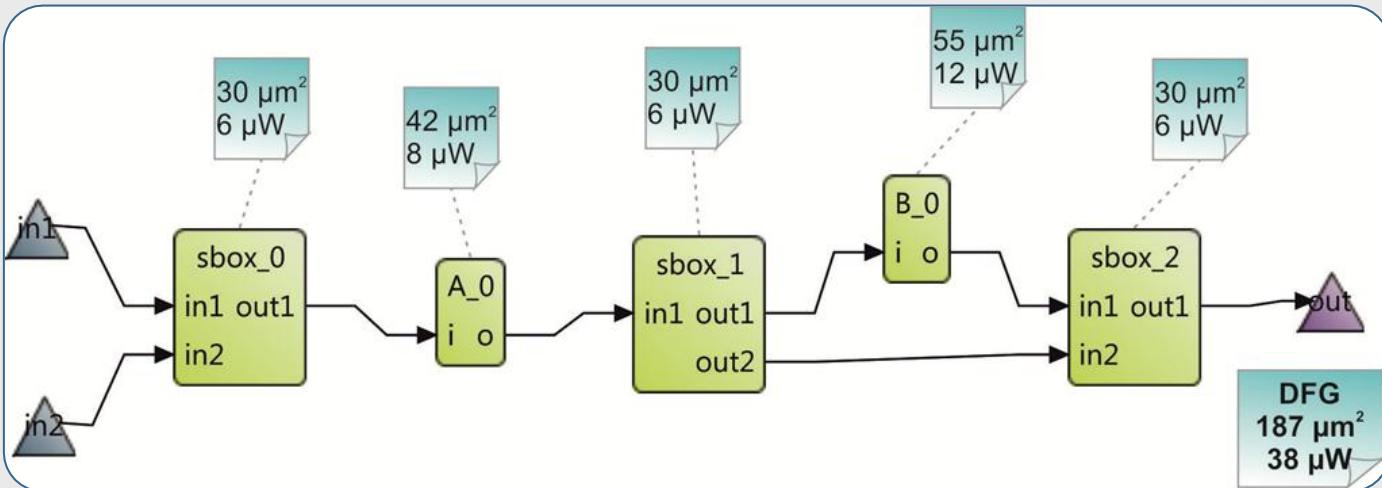
$V = \text{set of vertices} \quad v_i \in V$

$DFG = \langle V, E \rangle$

$E = \text{set of edges} \quad e_i \in E$

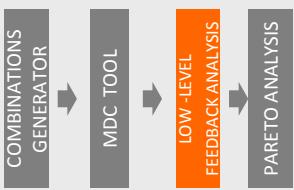
$$a_i = \text{Area}(v_i) \quad \rightarrow \quad \text{Area}(DFG) = \sum a_i$$

$$p_i = \text{Power}(v_i) \quad \rightarrow \quad \text{Power}(DFG) = \sum p_i$$

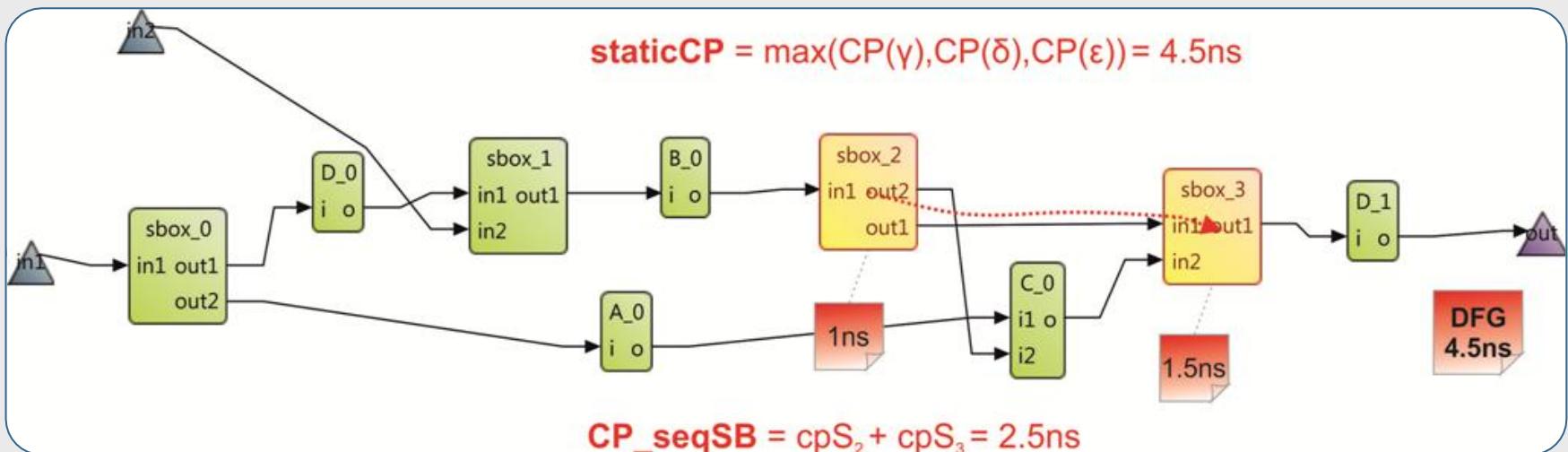
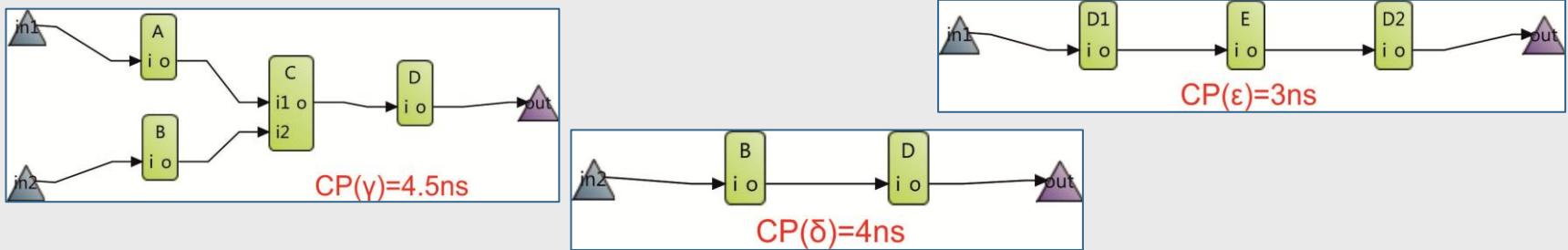




Low-level Feedback Analysis: frequency

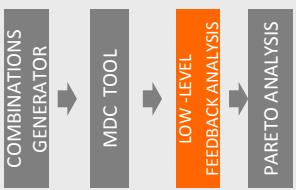


- $cpN_j = CP$ of the j -th SAD
→ $staticCP = \max(cpN_j)$
- $cpS_i = CP$ of the i -th Sbox
→ $CP_{seqSB} = \sum cpS_i$



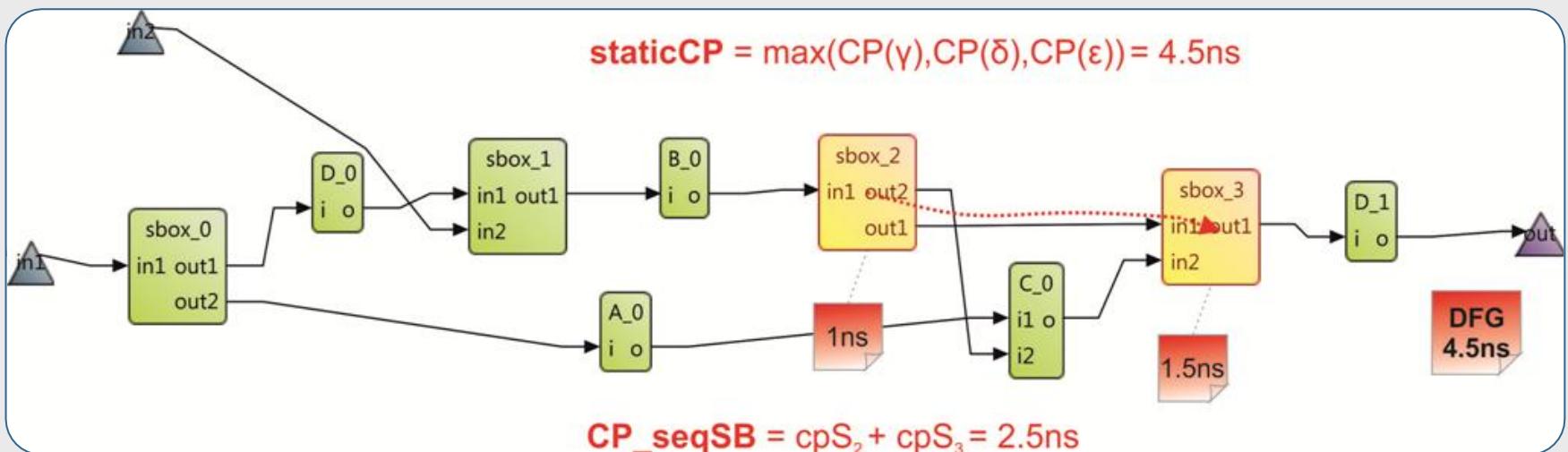
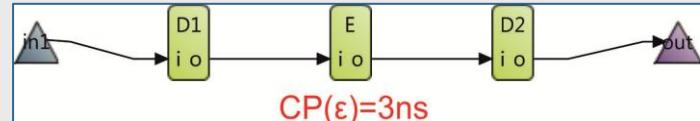
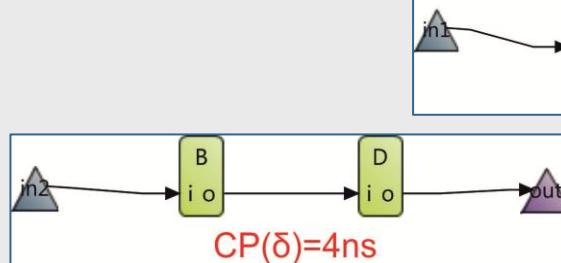
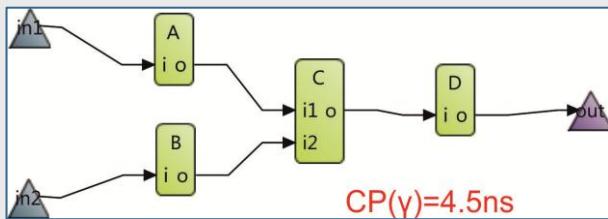


Low-level Feedback Analysis: frequency



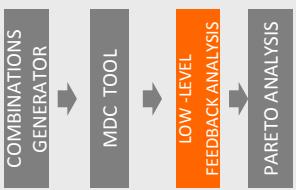
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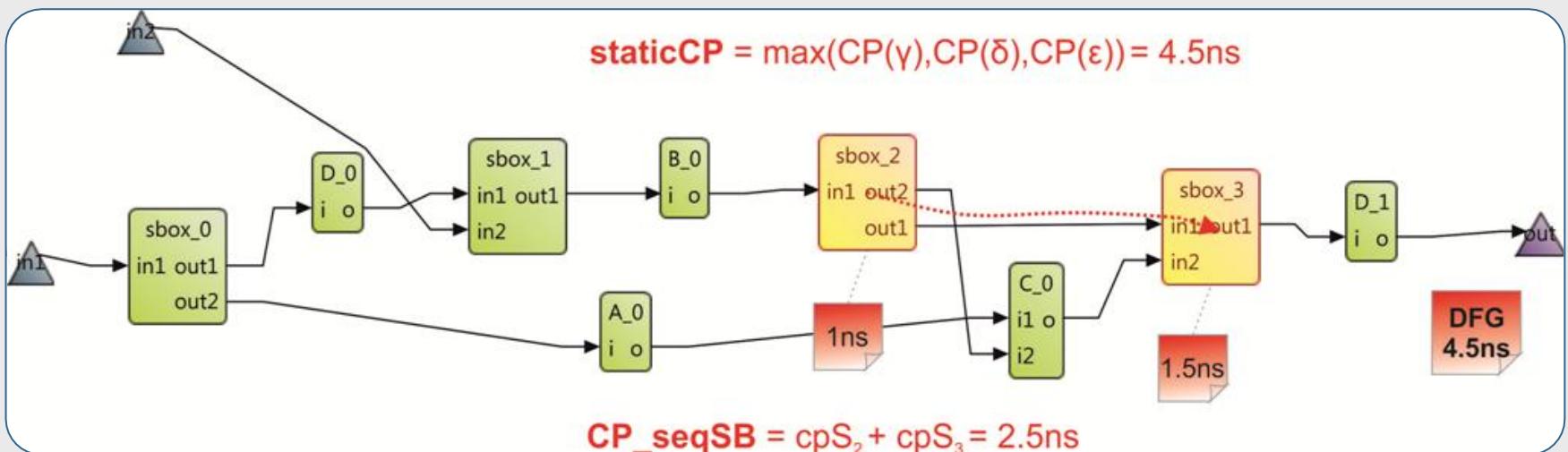
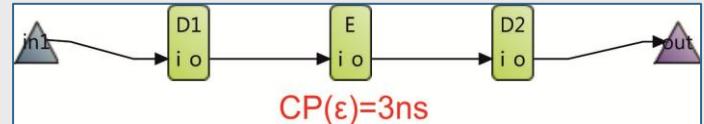
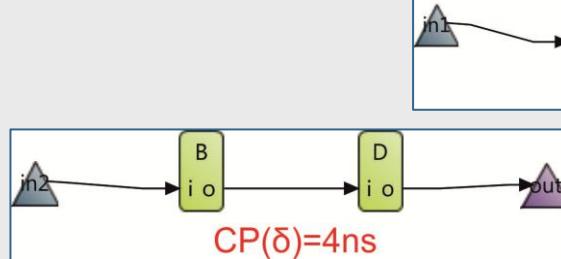
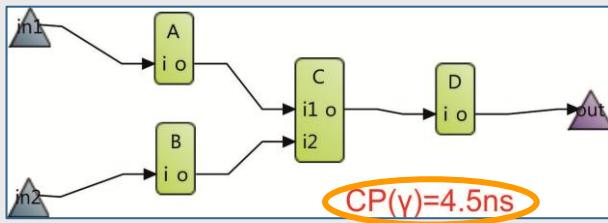


Low-level Feedback Analysis: frequency



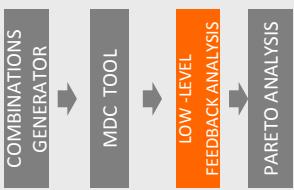
- $cpN_j = CP$ of the j -th SAD
 $\rightarrow \text{staticCP} = \max(cpN_j)$

- $cpS_i = CP$ of the i -th Sbox
 $\rightarrow CP_{\text{seqSB}} = \sum cpS_i$



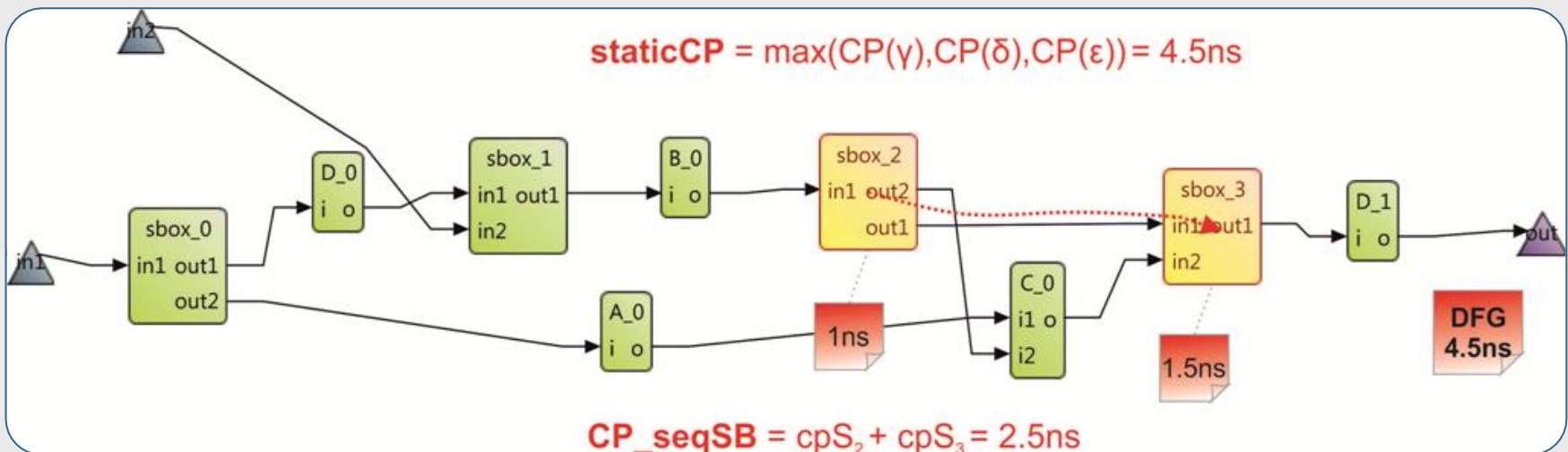
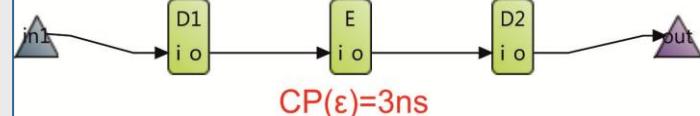
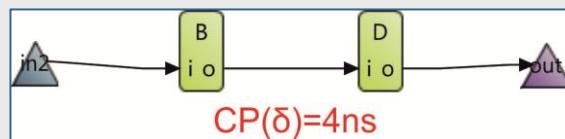
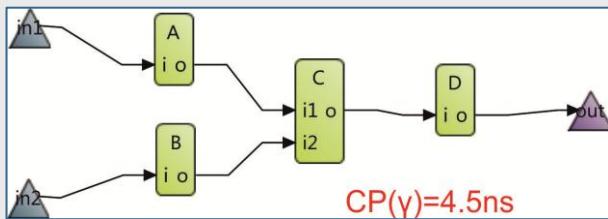


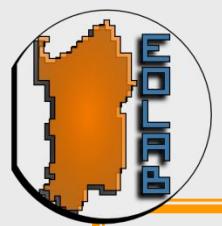
Low-level Feedback Analysis: frequency



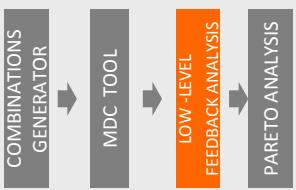
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- $cpS_i = CP$ of the i -th Sbox
 $\rightarrow \text{CP_seqSB} = \sum cpS_i$



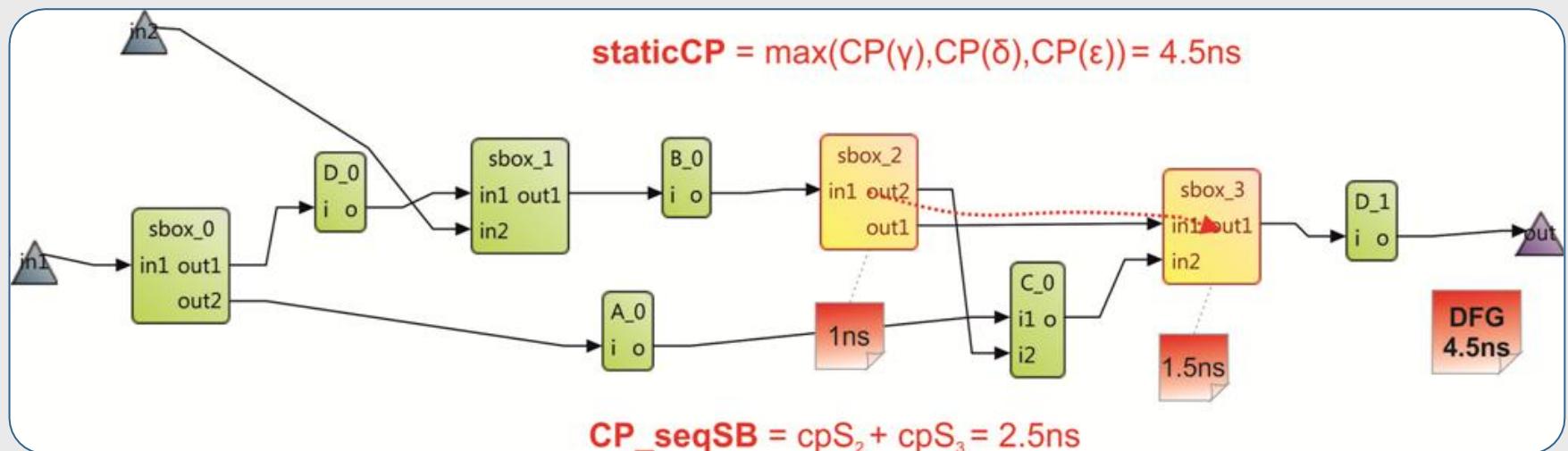
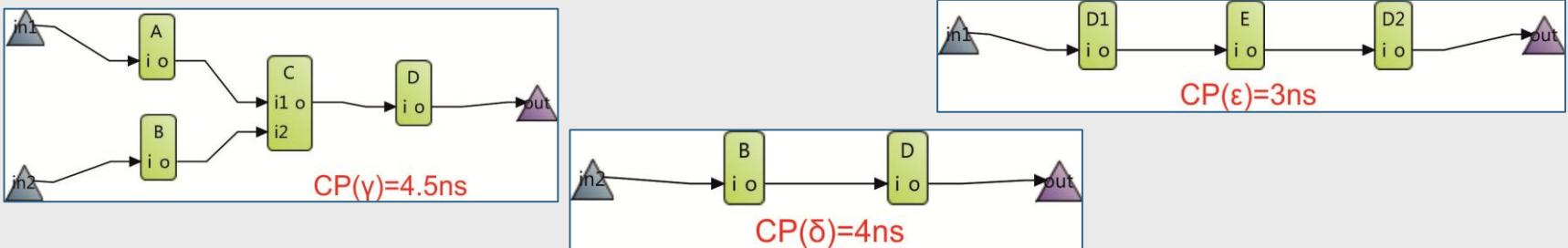


Low-level Feedback Analysis: frequency



- $cpN_j = CP$ of the j -th SAD
→ $staticCP = \max(cpN_j)$
- $cpS_i = CP$ of the i -th Sbox
→ $CP_{seqSB} = \sum cpS_i$

$$CP(DFG) = \max(Cpstatic, CP_{seqSB})$$

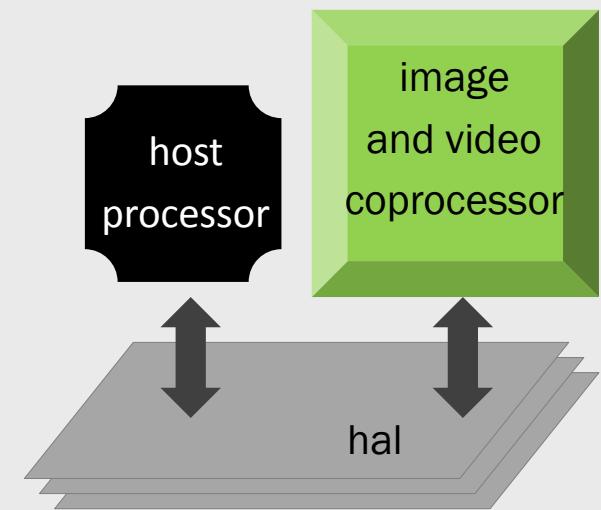




Design Under Test

Table: composition of the different analyzed use cases.

SADs	UC1	UC2	UC3
Qsort	X	-	X
Min_Max	X	X	X
Corr	X	-	X
Abs	X	X	X
Rgb2Ycc	X	-	X
Ycc2Rgb	X	-	X
Sbwlabel	-	X	X
Median	-	X	X
Cubic	-	X	X
Cubic_Conv	-	X	X
Check_GeneralBilevel	-	X	X



[F. Palumbo et.al., "The multi-dataflow composer tool: generation of on-the-fly reconfigurable platforms", in JrnL of Real Time Image Processing]

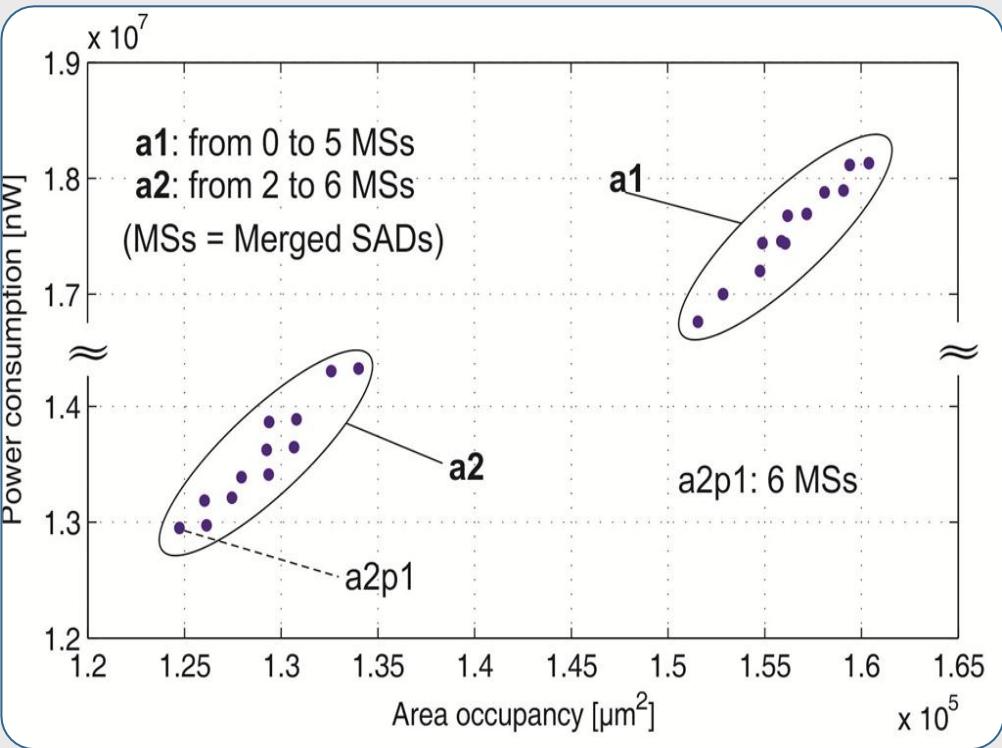
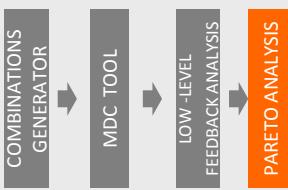
UC1: Antialiasing

UC2: Zoom

UC3: Antialiasing & Zoom



UC1 - Pareto Analysis



UC1: Antialiasing

Involved SADs:

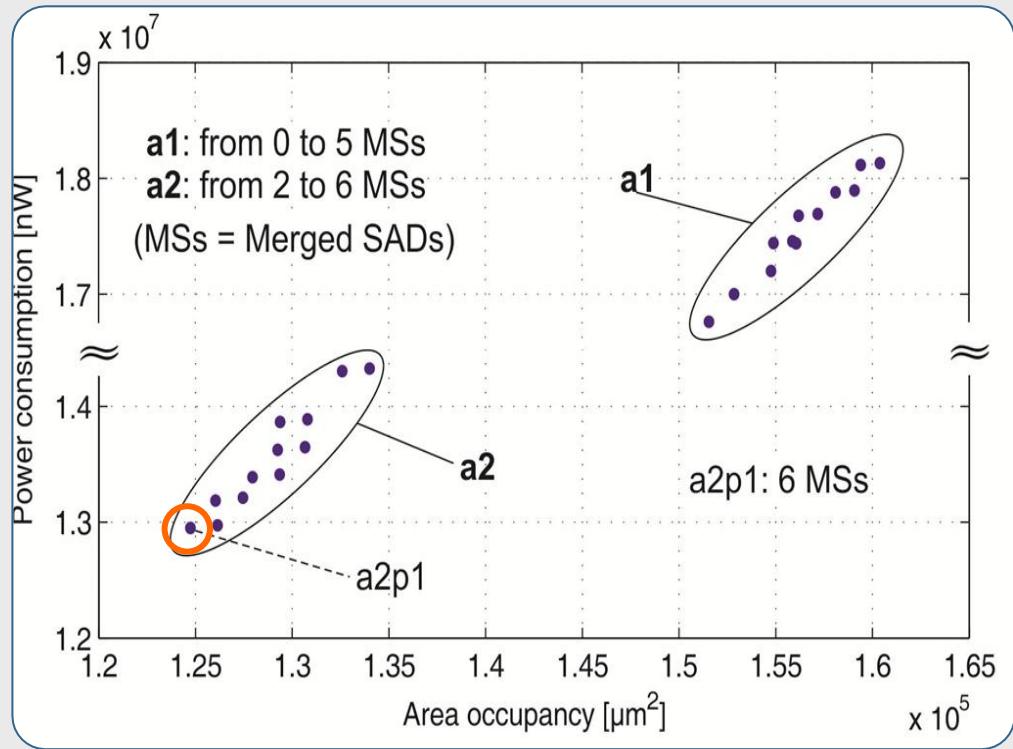
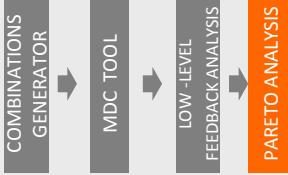
6

Design Space size:

1951 points



UC1 - Pareto Analysis



UC1: Antialiasing

Involved SADs:

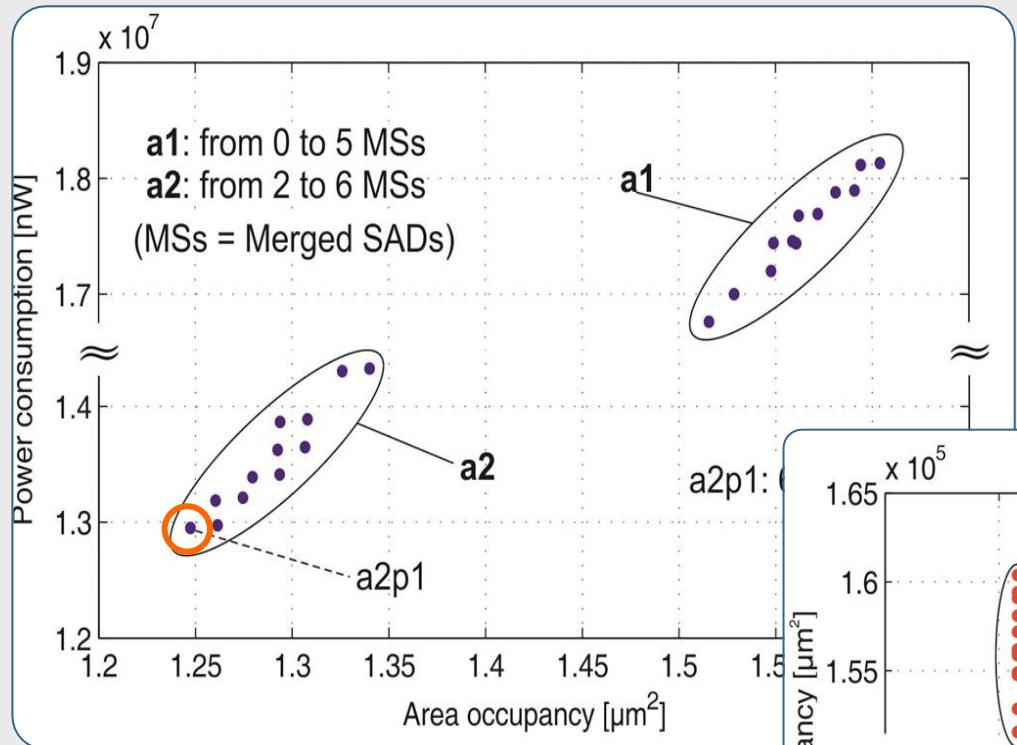
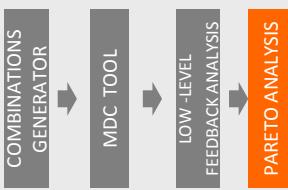
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Design Space size:

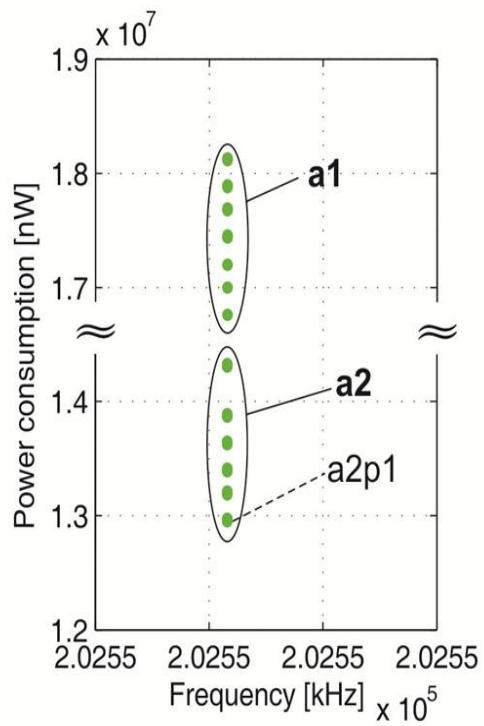
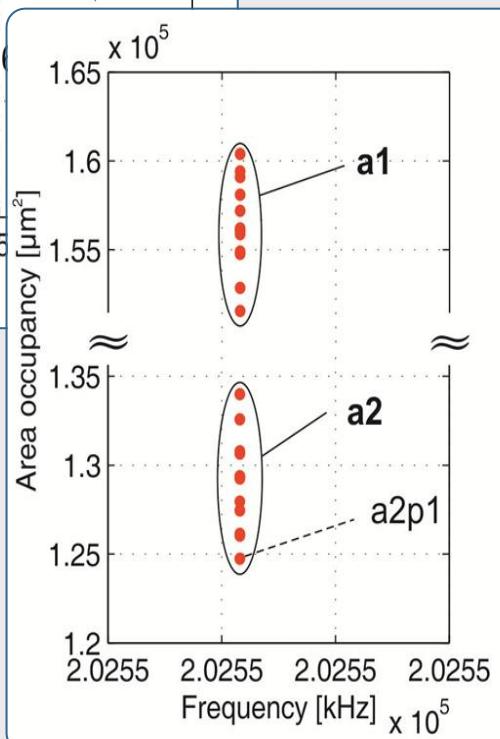
1951 points



UC1 - Pareto Analysis



UC1: Antialiasing



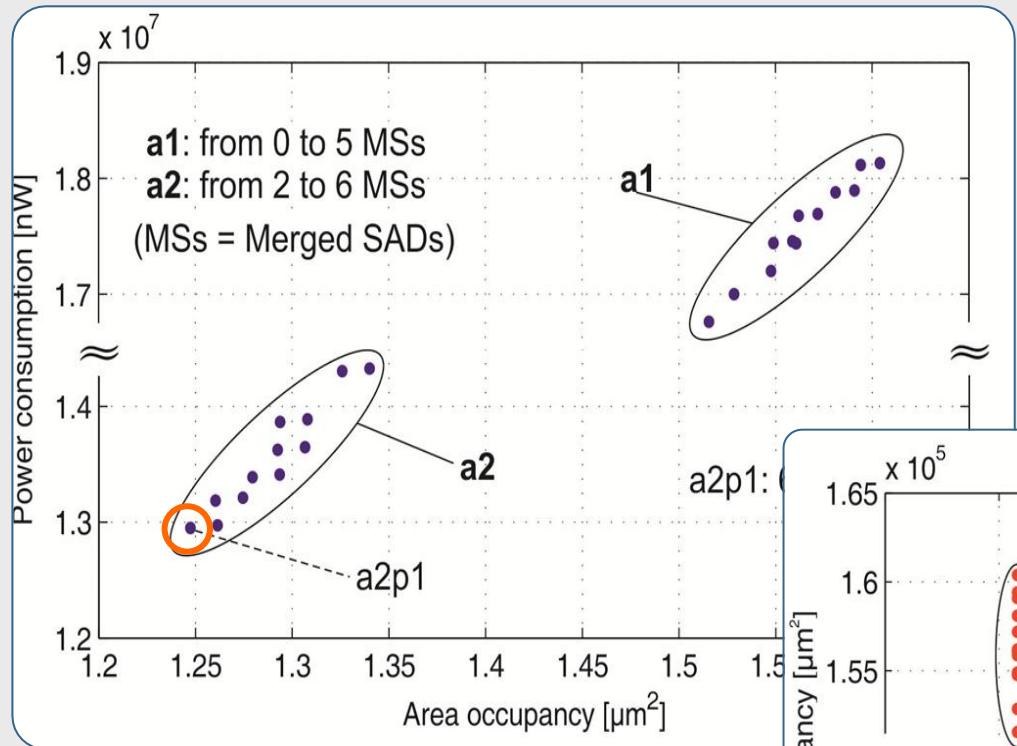
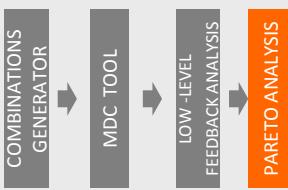
Involved SADs:

6

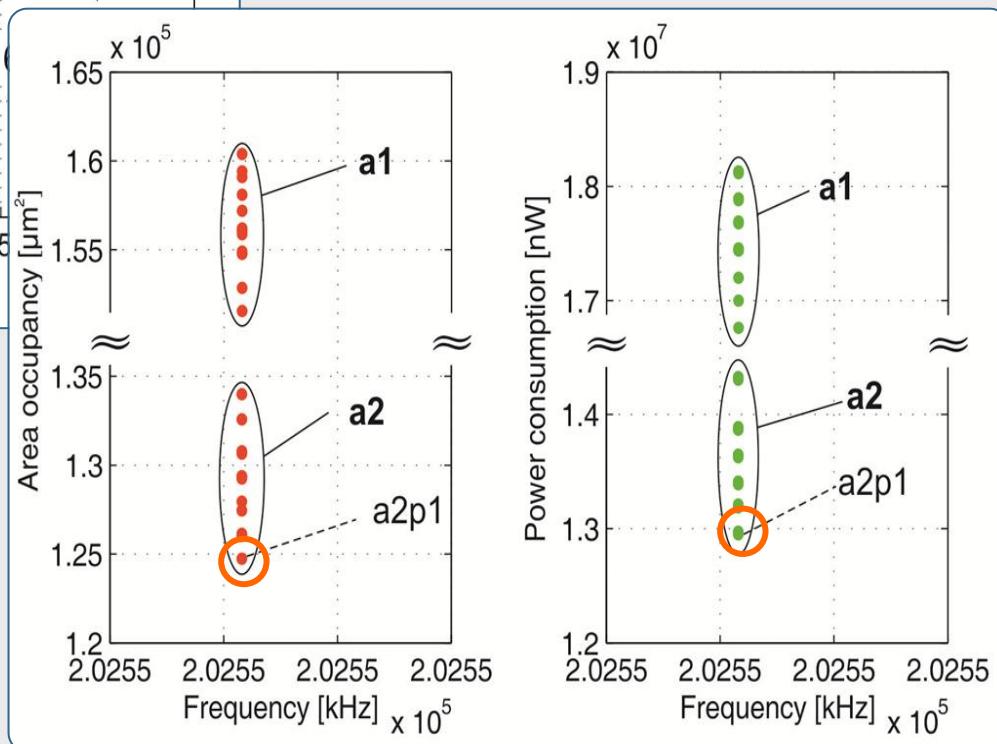
Design Space size:
1951 points



UC1 - Pareto Analysis



UC1: Antialiasing



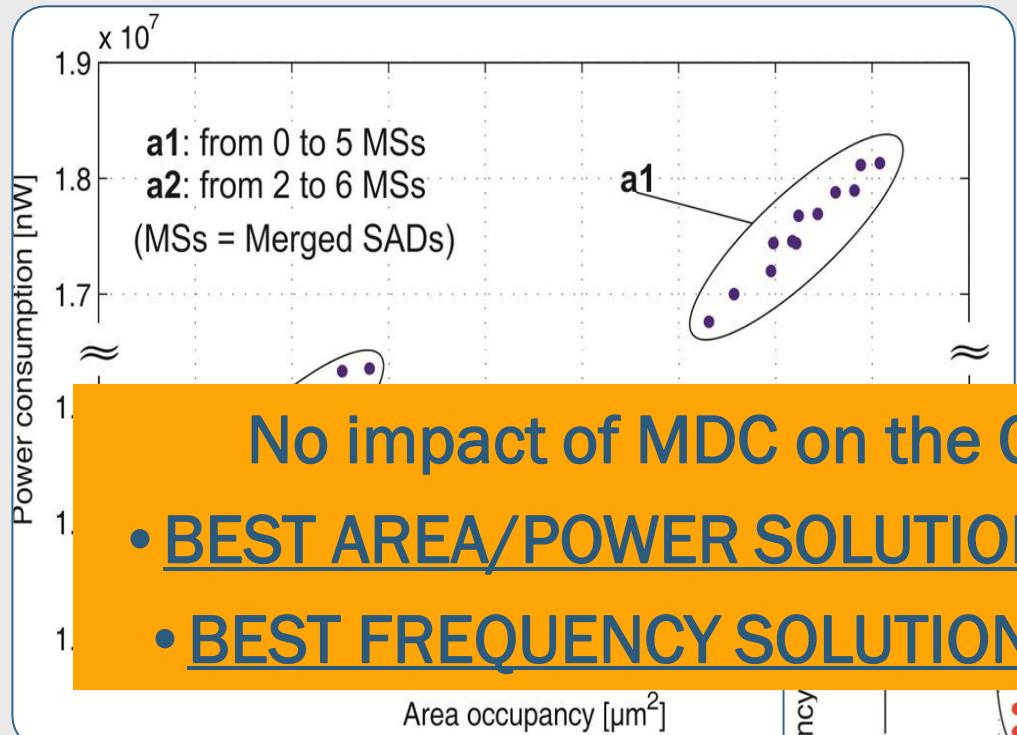
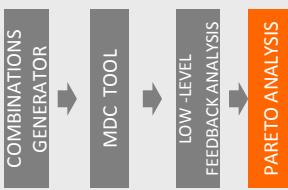
Involved SADs:

6

Design Space size:
1951 points



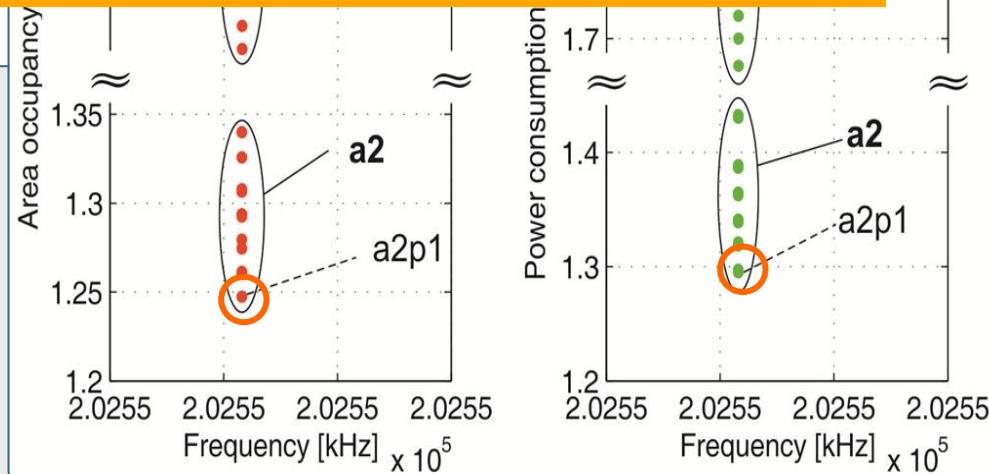
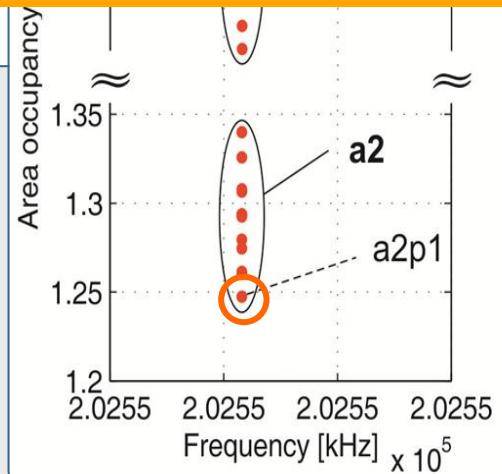
UC1 - Pareto Analysis



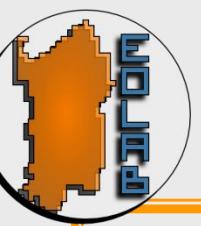
Involved SADs:

6

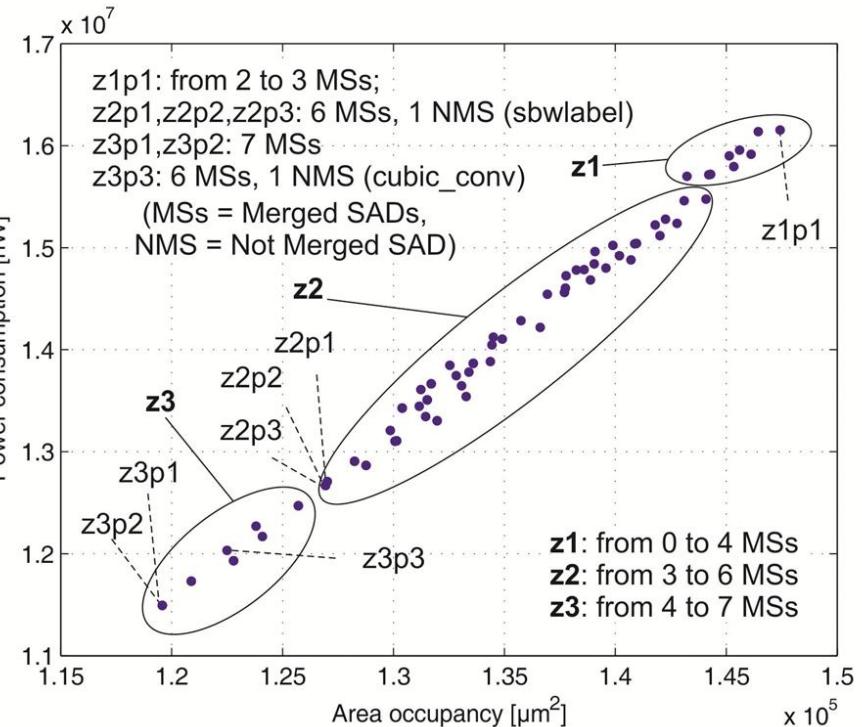
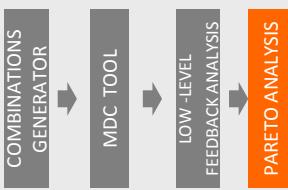
Design Space size:
1951 points



UC1: Antialiasing



UC2 - Pareto analysis



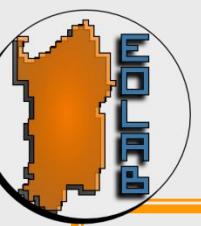
UC2: Zoom

Involved SADs:

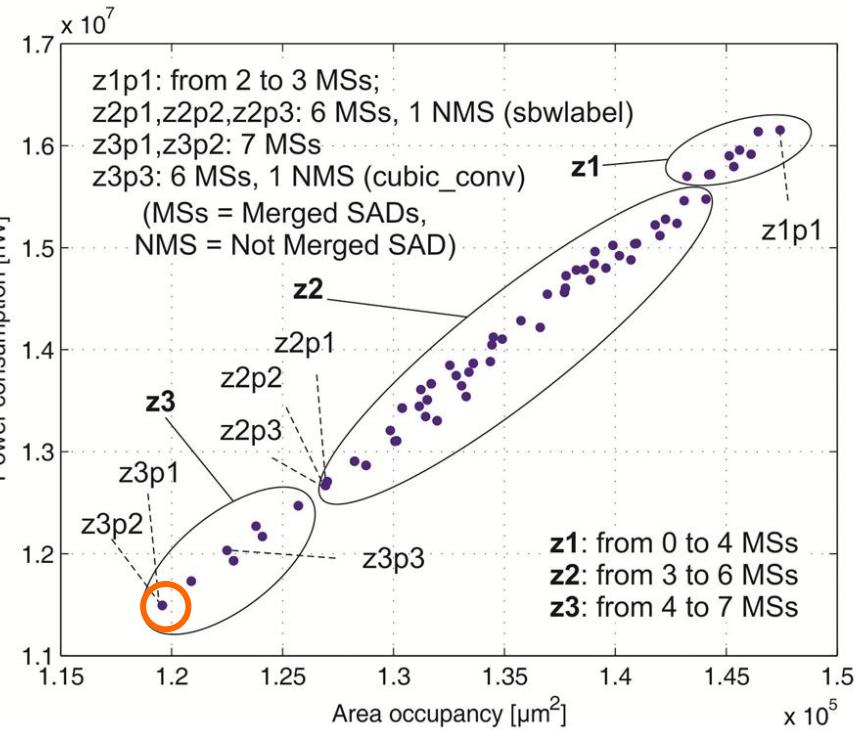
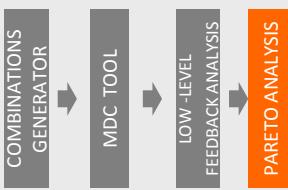
7

Design Space size:

13693 points



UC2 - Pareto analysis



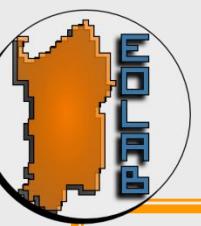
UC2: Zoom

Involved SADs:

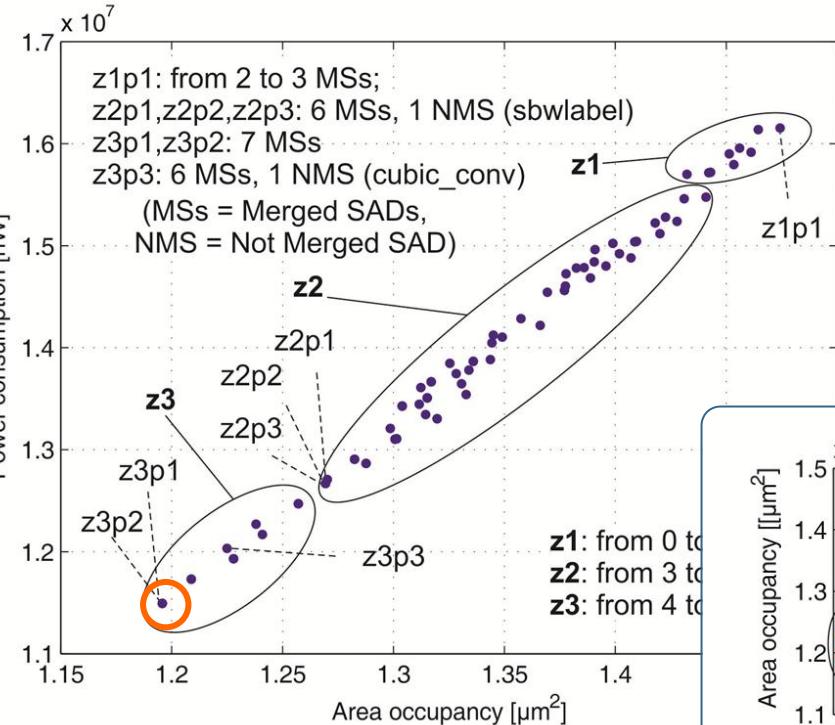
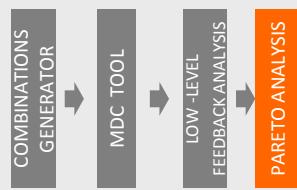
7

Design Space size:

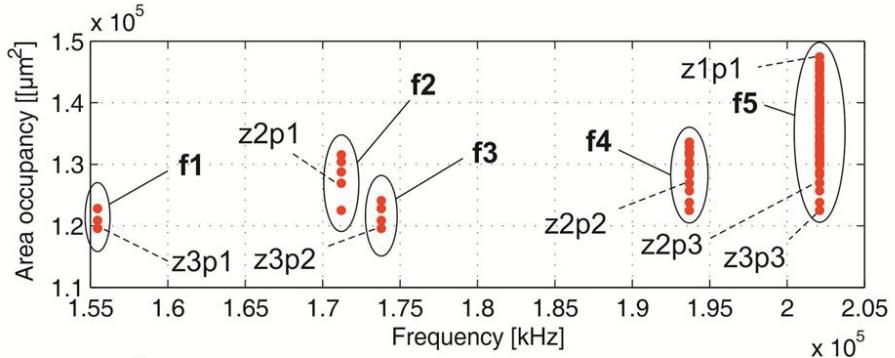
13693 points



UC2 - Pareto analysis



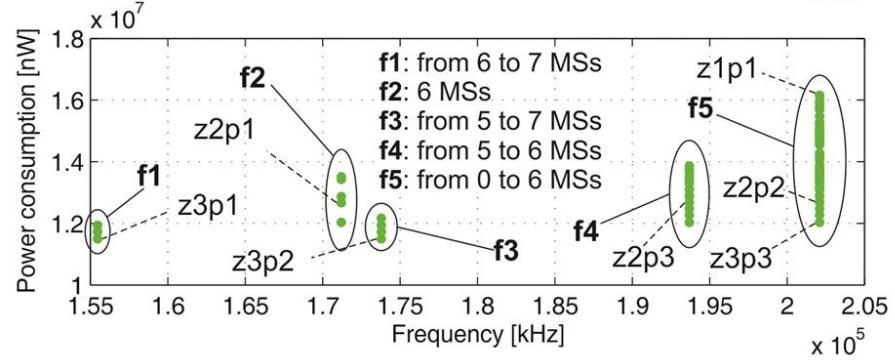
UC2: Zoom

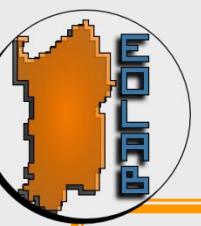


Involved SADs:

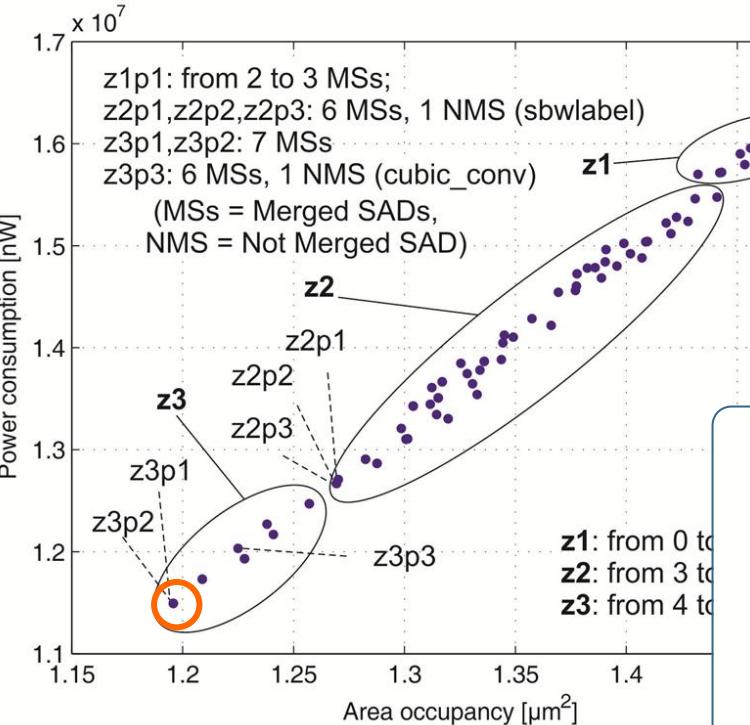
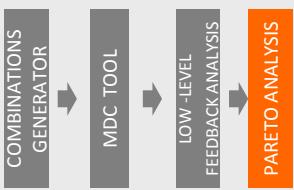
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Design Space size:
13693 points

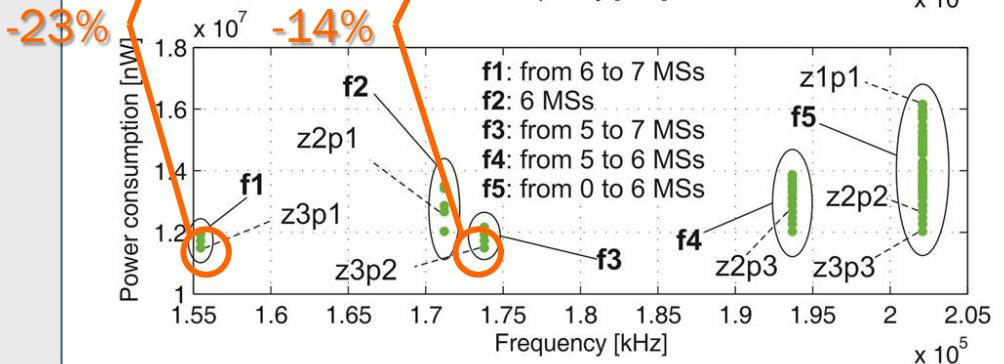
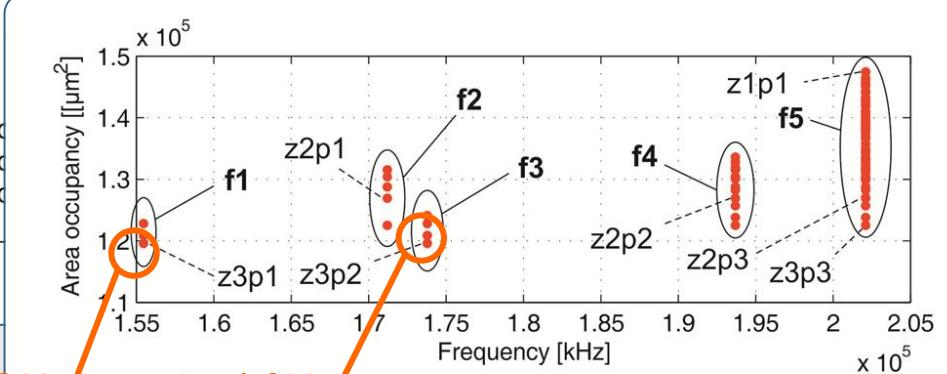




UC2 - Pareto analysis



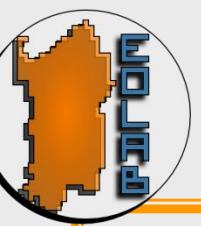
UC2: Zoom



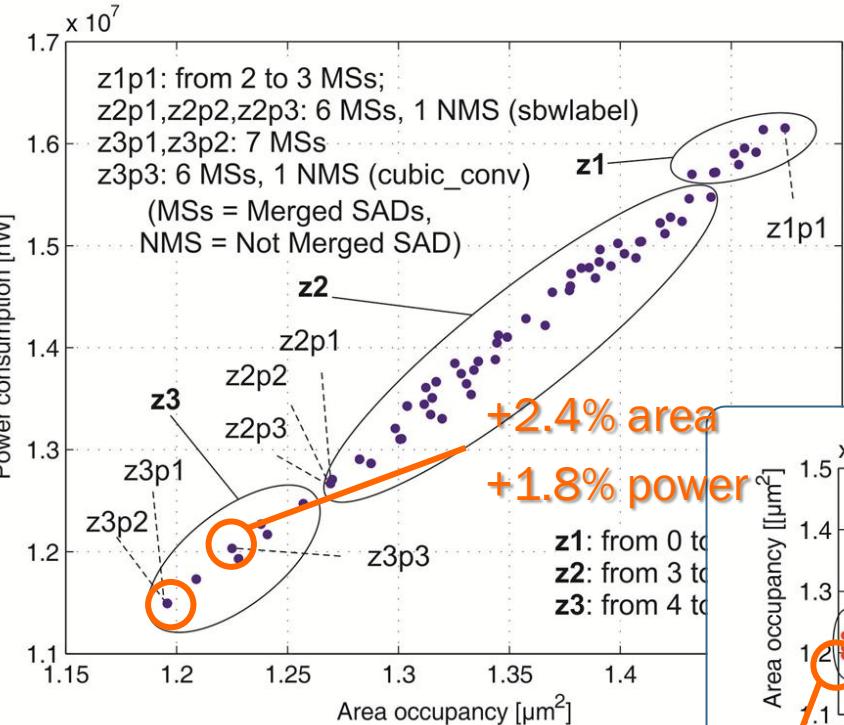
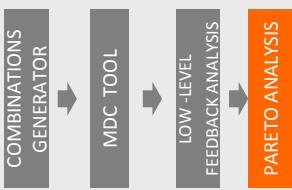
Involved SADs:

7

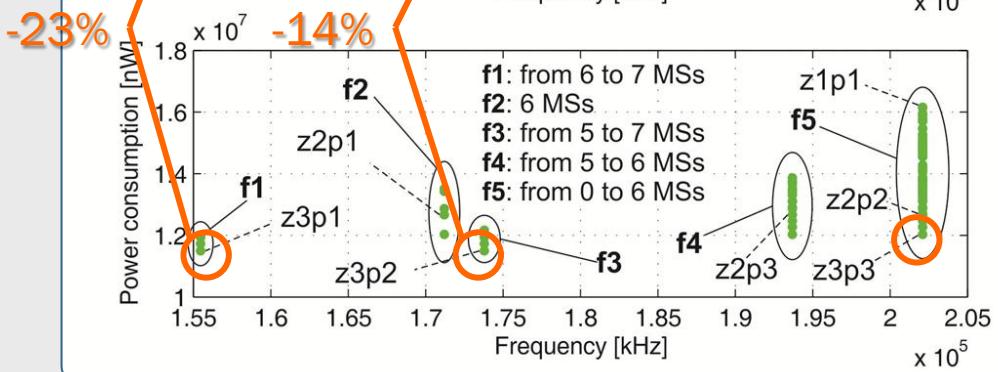
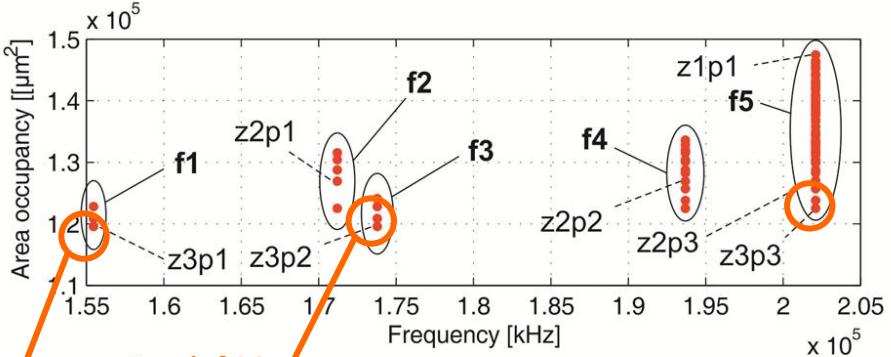
Design Space size:
13693 points



UC2 - Pareto analysis



UC2: Zoom



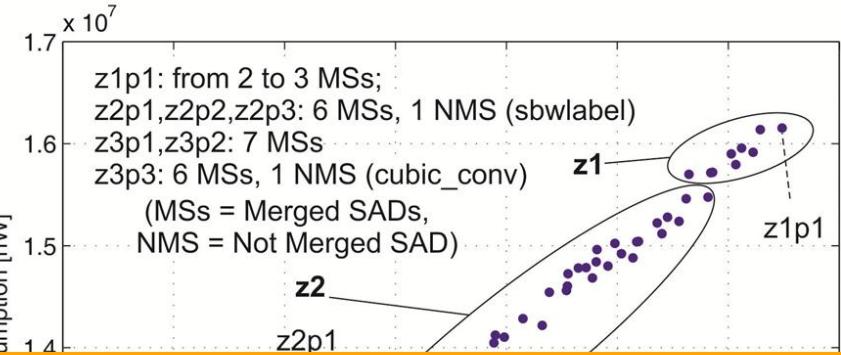
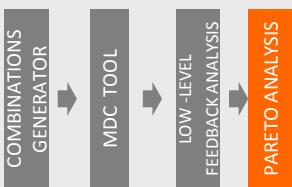
Involved SADs:

7

Design Space size:
13693 points



UC2 - Pareto analysis



UC2: Zoom

MDC impacts on the CP of the system

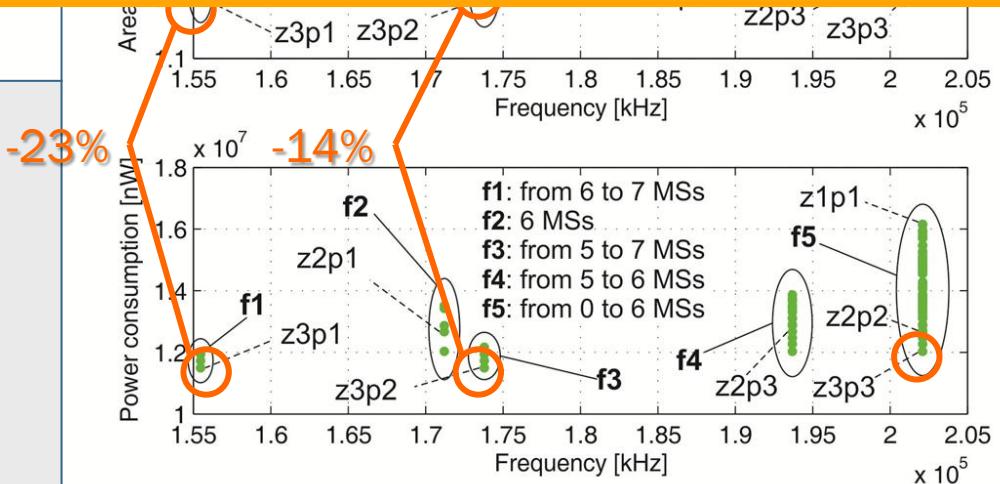
- BEST AREA/POWER SOLUTION: all merged (z3p1,z3p2)
- BEST FREQUENCY SOLUTION: hybrid, 6 merged SADs (z3p3)

Area occupancy [μm^2]

Involved SADs:

7

Design Space size:
13693 points





UC3 - Pareto analysis

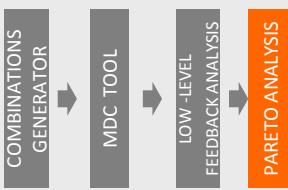


Table: percentage of the SAD overlapping actors with respect to an all merged solution.

SADs	UC1	UC2	UC3
Qsort	2,94%	-	1,89%
Min_Max	2,94%	3,12%	1,89%
Corr	11,76%	-	9,43%
Abs	2,94%	3,12%	1,89%
Rgb2Ycc	20,59%	-	15,09%
Ycc2Rgb	26,47%	-	18,87%
Sbwlabel	-	15,62%	11,32%
Median	-	18,75%	13,21%
Cubic	-	18,75%	11,32%
Cubic_Conv	-	9,38%	5,66%
Check_GeneratorBilevel	-	18,75%	11,32%

UC3: Antialiasing & Zoom

Involved SADs:

11

Design Space size:
108505101 points



UC3 - Pareto analysis

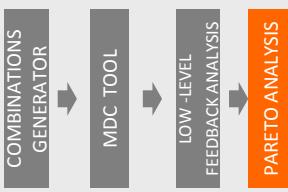


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Abs	2,94%	3,12%	1,89%
Rgb2Ycc	20,59%	-	15,09% ↗
Ycc2Rgb	26,47%	-	18,87% ↗
Sbwlabel	-	15,62%	11,32% ↗
Median	-	18,75%	13,21% ↗
Cubic	-	18,75%	11,32% ↗
Cubic_Conv	-	9,38%	5,66%
Check_GeneratorBilevel	-	18,75%	11,32% ↗

UC3: Antialiasing & Zoom

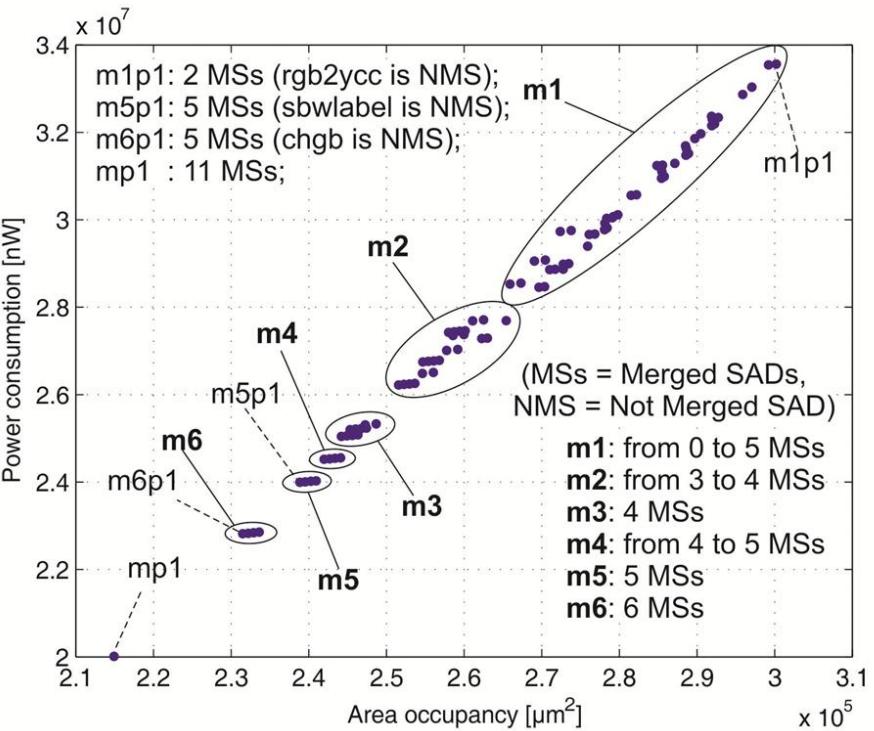
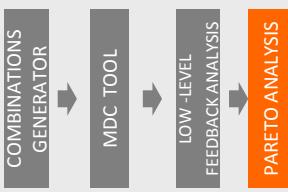
Involved SADs:

11

Design Space size:
108505101 points



UC3 - Pareto analysis



UC3: Antialiasing & Zoom

Involved SADs:

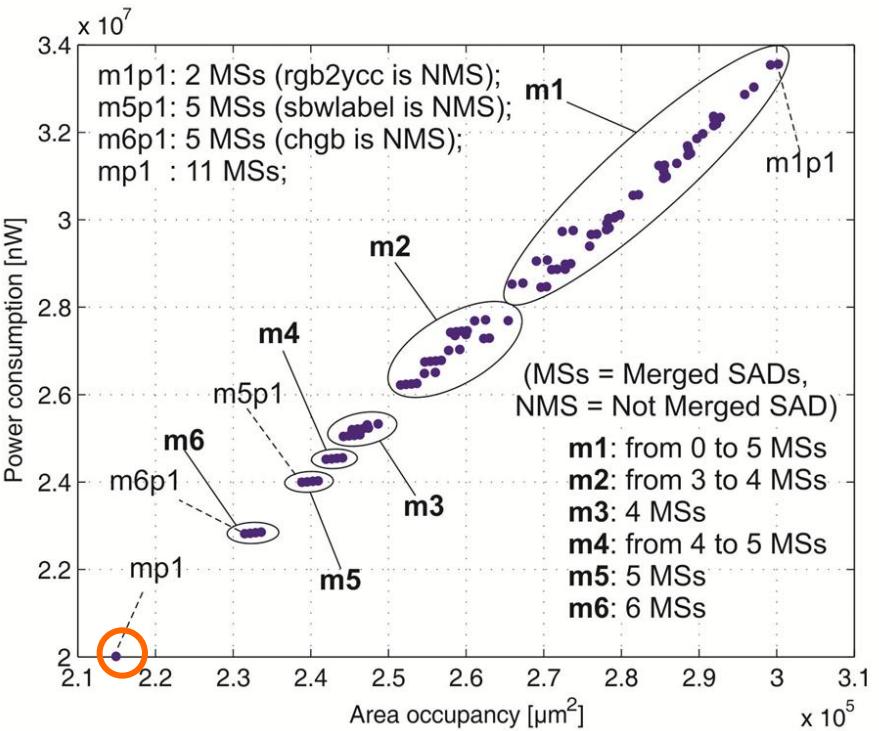
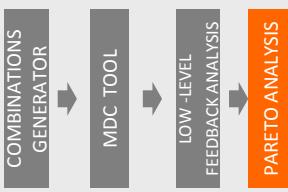
6 of 11

Design Subpace size:

1951 points



UC3 - Pareto analysis



UC3: Antialiasing & Zoom

Involved SADs:

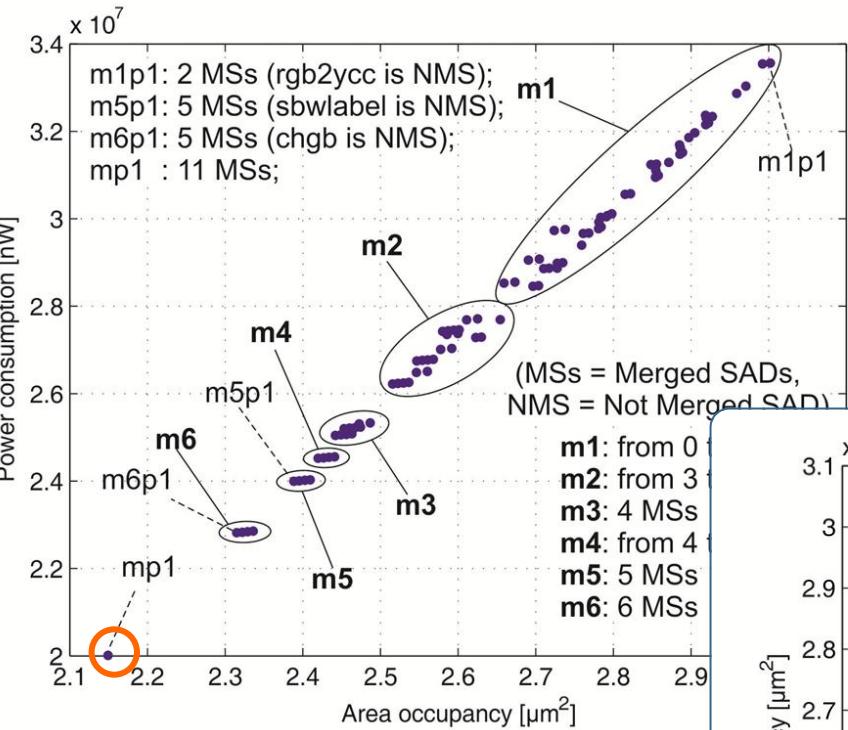
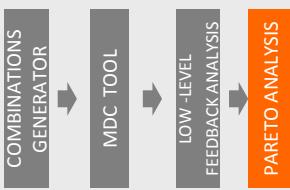
6 of 11

Design Subpace size:

1951 points



UC3 - Pareto analysis



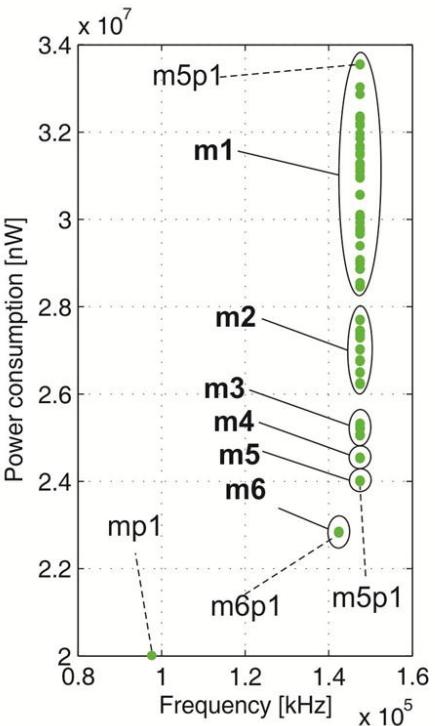
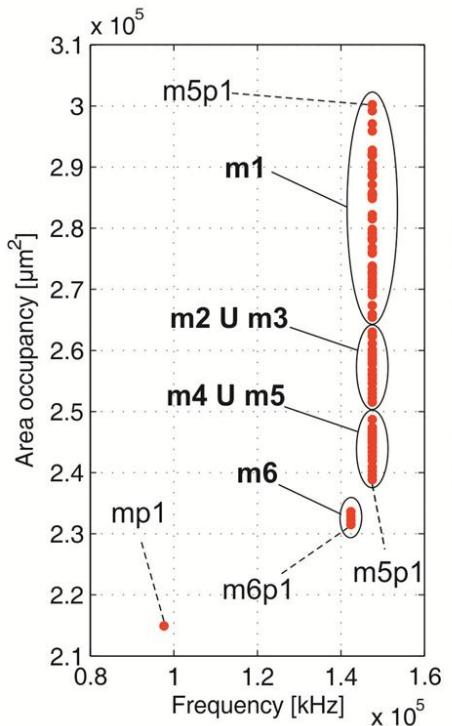
Involved SADs:

6 of 11

Design Subpace size:

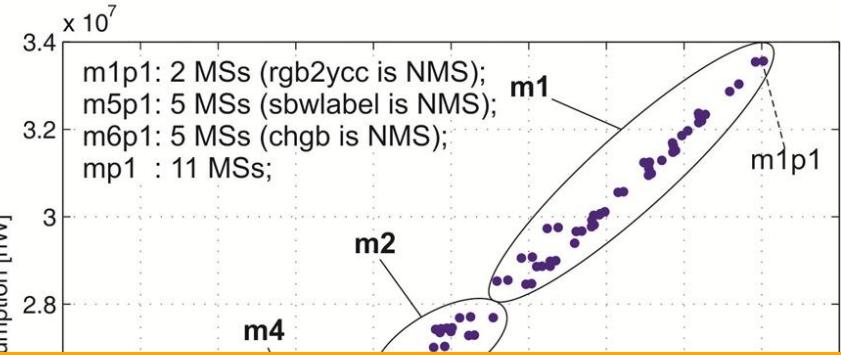
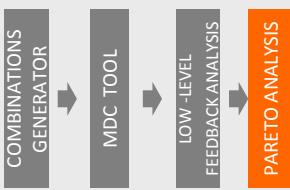
1951 points

UC3: Antialiasing & Zoom





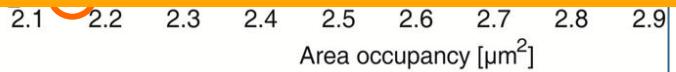
UC3 - Pareto analysis



UC3: Antialiasing & Zoom

Need of a heuristic if we have many SADs

- BEST AREA/POWER SOLUTION: heuristic only on all merged
- BEST FREQUENCY SOLUTION: affine proposed heuristic

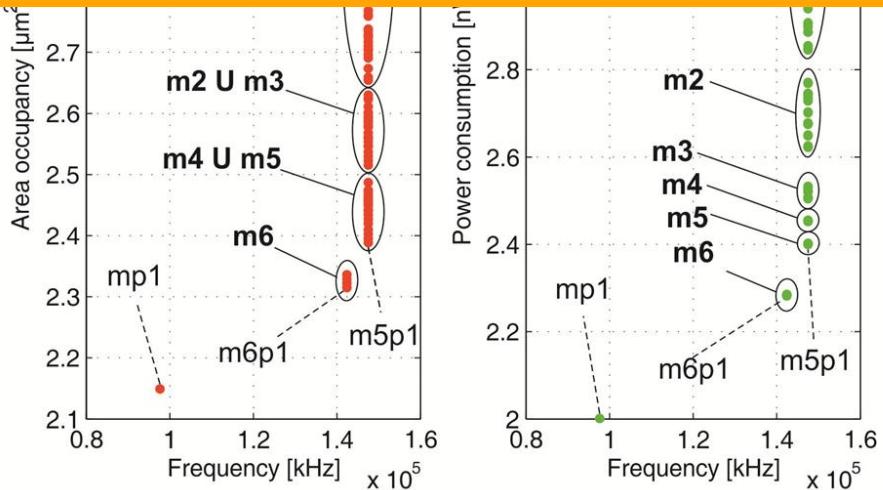


Involved SADs:

6 of 11

Design Subpace size:

1951 points





Final Remarks

- A DSE and a profiling methodology specifically conceived to guide designers targeting multi-context architectures has been presented:
 - The DSE and profiling are performed at a high level of abstraction, but back annotated low-level information are considered.
- Synthesis trials confirmed the applicability of the proposed methodology with an estimation error lower (on average) than the 7%.
 - Accuracy can be improved adopting more accurate parameterized models to compute the metrics of interest.
- Future developments will regard
 - Accuracy improvement
 - Introduction of automated clever heuristics, based on high-level information, to limit the dimension of the design space.



Acknowledgements

The research leading to these results has received funding from:



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under grant agreement CRP-18324
[RPCT Project]



the Region of Sardinia, Young
Researchers Grant, POR Sardegna FSE
2007-2013, L.R.7/2007 “Promotion of
the scientific research and
technological innovation in Sardinia”
under grant agreement CRP-18324
RPCT Project

8th International Symposium on Image and Signal Processing and Analysis - 2013
Special Session on Hardware-software Co-design Methodologies for Streaming
Processing in Digital Media Technologies



**September 4th-6th, 2013,
Trieste, Italy**



DSE and Profiling of Multi-Context Coarse-Grained Reconfigurable Systems



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