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Multi-Purpose Systems: A Novel DataFlow-Based Generation and Mapping Strategy

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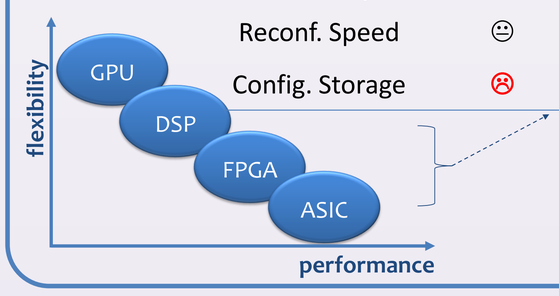
Reconfigurable architectures

Reconfigurable architectures are specialized computing platforms capable of changing configuration to serve the targeted computations.

	fine-grained (bit level)	Coarse-grained (word level)
Flexibility	☺	😐
Reconf. Speed	😐	☺
Config. Storage	☹	😐



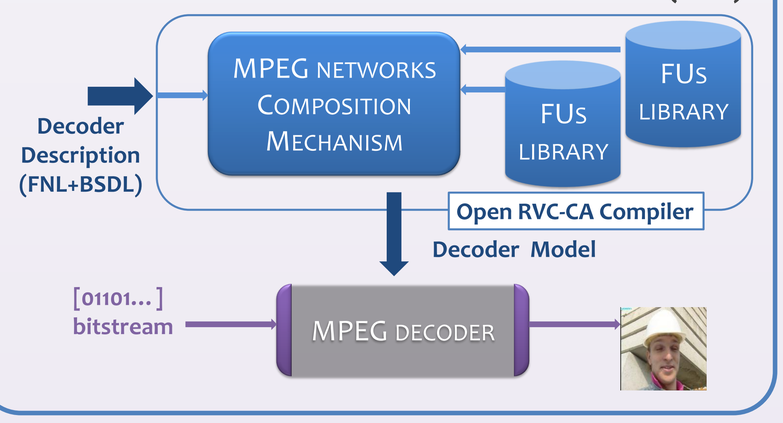
Introduction

Manual creation of hardware designs for multi-purpose systems has always required a lot of effort in addition to being error-prone and time-consuming.

To tackle these issues, we propose a novel design flow based on the Dataflow Process Networks Model of Computation that combine two tools: the Multi-Dataflow Composer and the Open RVC-CAL Compiler. Our approach guarantees runtime efficiency and on-chip area saving both on FPGAs and ASICs.

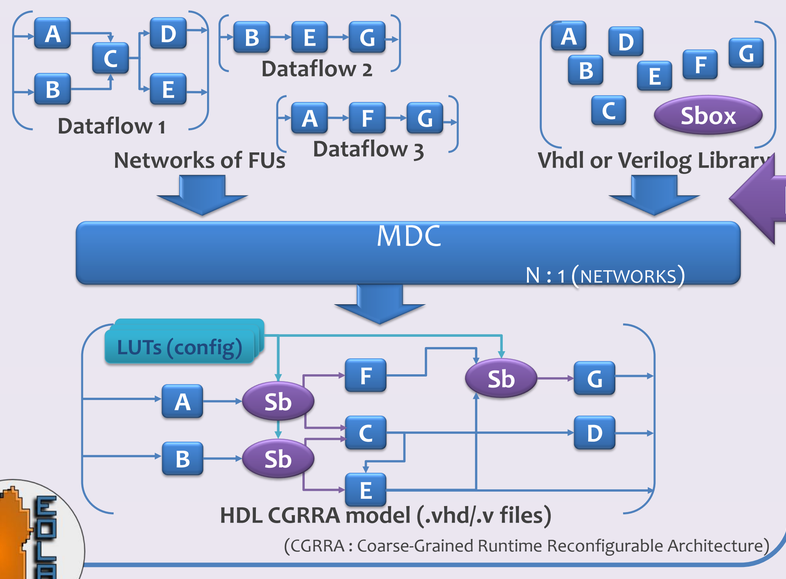
Reconfigurable Video Coding (RVC)

RVC is an MPEG standard that gives the possibility of specifying video decoders as dataflow programs (networks) composed of functional units (FUs).



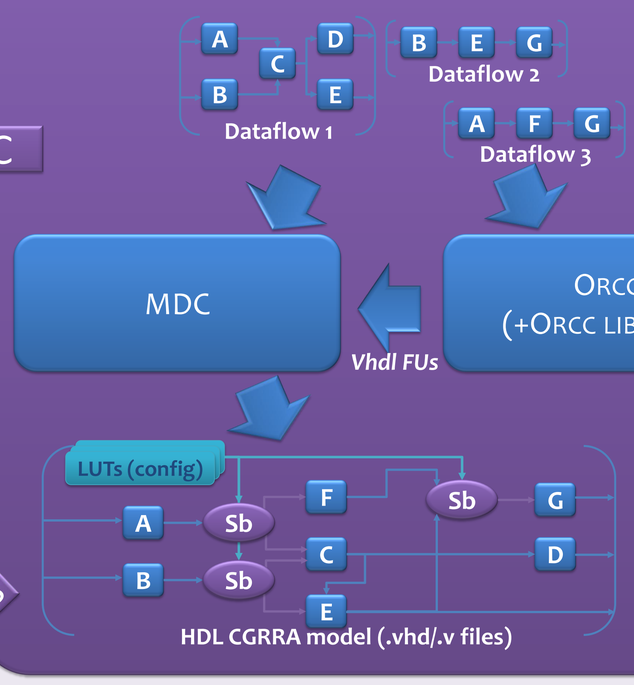
Multi-Dataflow Composer (MDC)

MDC handles the automatic mapping of dataflow programs into a reconfigurable multi-purpose substrate



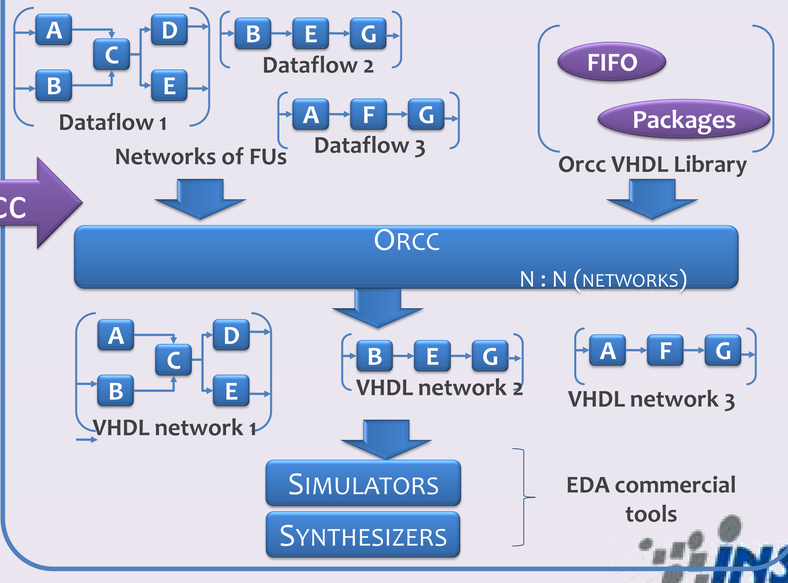
Novel dataflow-based design flow

The novel design flow allows multiple D-MoC models to be mapped as coarse-grained reconfigurable hardware.



Open RVC-Cal Compiler (Orcc - VHDL)

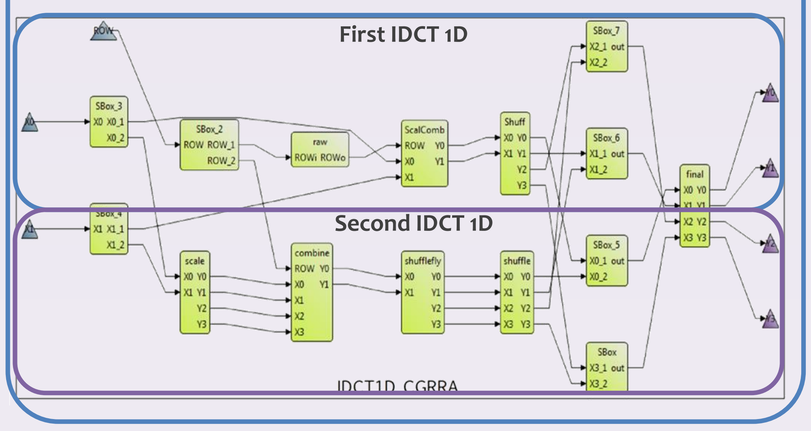
Orcc handles the compilation of RVC functional units into efficient, understandable, and multi-target VHDL code



IDCT 1D use-case

This RVC program is a proof concept: starting from two IDCT1D and automatically generate a CGRRA model

FPGA: 5% area-saving (one actor shared: Final) and same frequency / throughputs.



Conclusion

Promising results have been achieved both on FPGAs and ASICs, resulting in 30% and 40% area savings respectively, at a negligible frequency penalty.

This dataflow-based design flow contributes to close the gap between hardware and software, automatically mapping complex software applications on various hardware platforms. Flexibility and specialization needs are met exploiting a coarse-grained RP.

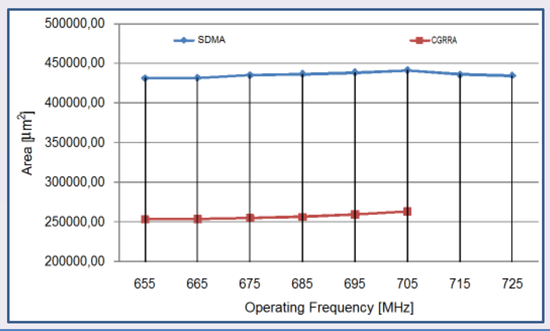
IDCT 2D use-case

This RVC program is a complex application that highlight the results of our approach

	SDMA	CGRRA	+/-
F [MHz]	116	114	+1.7
# Slices	2462	1666	-32.3
#LUTs	2465	1894	-12.2
P [mW]	409	401	-2

Xilinx Virtex6

90nm CMOS



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