A Coarse-Grained Reconfigurable Wavelet Denoiser Exploiting the Multi-Dataflow Composer Tool

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Introduction

- Some application-specific fields, such as the biomedical one, push towards **area**- and **power**- effective VLSI implementation of digital signal processing algorithms mainly for the development of wearable or implantable devices.

- To this aim, the **Multi-Dataflow Composer** (MDC) tool, originally conceived for image/video processing, can be exploited in other domains leading to optimal hardware implementations.

- The MDC-based hardware platforms are **flexible**, fitting to parametric solutions adjustable at runtime, according to the characteristics of the signal of interest.
Research goals

- Exploit strategies of resources **reusability** through **reconfiguration** to provide area and power minimization.

- Demonstrate the potential **orthogonality** of the MDC approach with respect to the Reconfigurable Video Domain (RVC) domain.

- Test the proposed approach on a runtime reconfigurable **Wavelet Denoiser**, targeted for biomedical applications, prototyped onto an **FPGA** Development Board.

- Evaluate benefits in terms of **area** and **power** in comparison to traditional solutions and verify the system functionality using simulated datasets of neural signals.
Multi-Kernel Datapath Generation

HDL Components library, the *Functional Units* (FUs) implementing the actors:
- IEEE 754-1985 compliant arithmetic modules;
- control flow modules.
All the FUs obey to the same FIFO-based communication protocol.

Global Kernel
a Coarse-Grained Reconfigurable Hardware Platform with the minimum number of FUs
Use Case: Wavelet Denoising (WD)

- WD aims at **removing** the **background noise** corrupting the signal of interest, especially when it can be modeled as a Gaussian-distributed random noise.

- Translation Invariant solution: à-trous algorithm implementation.

- The number of Decomposition/Recomposition levels depends on the chosen input frequency and on the spectral characteristics of both noise and signal of interest.

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A pair of quadrature mirror Finite Impulse Response (FIR) filters at each level
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Registers to balance the delay of each path of the trellis
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Translation Invariant solution: à-trous algorithm implementation.

Band-Pass solution

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WD: thresholding phase

- To minimize the hardware resources, an **hard thresholding** has been implemented: only samples with values greater than $\theta$ are passed whereas the others are cleared to zero.

- $\theta$ can coincide with a scaled version of the standard deviation $\sigma_n$ of the additive noise source, computed iteratively analysing consecutive windows of $b_{\_len}$ detail samples.

$$th = SC \cdot \sigma_{2^j} = 3.9 \sqrt{\frac{1}{4 \cdot b_{\_len} - 1} \sum_{n=1}^{4} s_{n,2^j}}$$

$$s_{n,2^j} = \sum_{k=0}^{b_{\_len}} d_{2^j}[k]$$
Considering an input sampling frequency of 12kHz, 4 levels of decomposition/recomposition and removing the approximation signal at the 4th level, the denoised signal has a bandwidth between 375Hz and 6kHz.

Different computational kernels can be identified for the MDC tool. They should present commonalities at the actor level, enabling reuse of common hardware FUs.
Computing Kernels

dec kernel
Computing Kernels

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Computing Kernels

thr kernel

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Test Environment

To evaluate the MDC-based wavelet denoiser functionality, a processor-coprocessor system has been designed and implemented on a Xilinx FPGA Spartan-3E 1600 Development Board.
For every new input buffer frame of $b_{len}$ samples:

```
Decomposition
Begin
  $d_{21}[n] \leftarrow \text{copr\_dec\_level\_1}(\text{in\_data}, H(z), G(z), b_{len})$
  $d_{22}[n] \leftarrow \text{copr\_dec\_level\_2\_no\_coeff}(b_{len})$
  $d_{23}[n] \leftarrow \text{copr\_dec\_level\_3\_no\_coeff}(b_{len})$
  $d_{24}[n] \leftarrow \text{copr\_dec\_level\_4\_no\_coeff}(b_{len})$
End

Thresholding
Recomposition
Begin
  if cut $a_{24}[n]$ then
    \text{copr\_rec\_level\_4}(\text{Zero\_coeffs}, G'(z), b_{len})
    \text{copr\_rec\_level\_3}(H'(z), G'(z), b_{len})
  else
    \text{copr\_rec\_level\_4}(H'(z), G'(z), b_{len})
    \text{copr\_rec\_level\_3\_no\_coeff}(b_{len})
  end if
  \text{copr\_rec\_level\_2\_no\_coeff}(b_{len})
  \text{den\_data\_block} \leftarrow \text{copr\_rec\_level\_1\_no\_coeff}(b_{len})
End
```
For every new input buffer frame of $b\_len$ samples:

Decomposition

Begin

\[ d_{21}[n] \leftarrow \text{copr\_dec\_level\_1}(\text{in\_data}, H(z), G(z), b\_len) \]
\[ d_{22}[n] \leftarrow \text{copr\_dec\_level\_2\_no\_coeff}(b\_len) \]
\[ d_{23}[n] \leftarrow \text{copr\_dec\_level\_3\_no\_coeff}(b\_len) \]
\[ d_{24}[n] \leftarrow \text{copr\_dec\_level\_4\_no\_coeff}(b\_len) \]

end

Thresholding

Recomposition

Begin

If cut $a_{24}[n]$ then

\[ \text{copr\_rec\_level\_3}(\text{Zero\_coeffs}, G'(z), b\_len) \]
\[ \text{copr\_rec\_level\_4}(H'(z), G'(z), b\_len) \]

else

\[ \text{copr\_rec\_level\_4}(H'(z), G'(z), b\_len) \]
\[ \text{copr\_rec\_level\_3\_no\_coeff}(b\_len) \]
end if

\[ \text{copr\_rec\_level\_2\_no\_coeff}(b\_len) \]
\[ \text{den\_data\_block} \leftarrow \text{copr\_rec\_level\_1\_no\_coeff}(b\_len) \]

end
For every new input buffer frame of \( b_{\text{len}} \) samples:

- **Decomposition**
  - **Begin**
  - \( d_{21}[n] \leftarrow \text{copr\_dec\_level\_1}(\text{in\_data}, H(z), G(z), b_{\text{len}}) \)
  - \( d_{22}[n] \leftarrow \text{copr\_dec\_level\_2\_no\_coeff}(b_{\text{len}}) \)
  - \( d_{23}[n] \leftarrow \text{copr\_dec\_level\_3\_no\_coeff}(b_{\text{len}}) \)
  - \( d_{24}[n] \leftarrow \text{copr\_dec\_level\_4\_no\_coeff}(b_{\text{len}}) \)
  - **end**

- **Thresholding**
  - **Recomposition**
  - **Begin**
  - if cut \( a_{24}[n] \) then
    - \( \text{copr\_rec\_level\_4}(\text{Zero\_coeffs}, G'(z), b_{\text{len}}) \)
    - \( \text{copr\_rec\_level\_3}(H'(z), G'(z), b_{\text{len}}) \)
  - else
    - \( \text{copr\_rec\_level\_4}(H'(z), G'(z), b_{\text{len}}) \)
    - \( \text{copr\_rec\_level\_3\_no\_coeff}(b_{\text{len}}) \)
  - end if
  - \( \text{copr\_rec\_level\_2\_no\_coeff}(b_{\text{len}}) \)
  - \( \text{den\_data\_block} \leftarrow \text{copr\_rec\_level\_1\_no\_coeff}(b_{\text{len}}) \)
  - **end**
The implemented coprocessor is highly **parametric**. The designer can choose at runtime:

- the number $N$ of levels used in decomposition/recomposition;
- the number and the values of the coefficients used for the FIR filters;
- the possibility of removing the last *approximation* signal to obtain a band-pass filtering;
- the threshold values for the *details* at each decomposition level;
- the $b_{len}$ number of samples for each input frame (allowable maximum: 512).

The input signal can be applied in input to the testing environment through an UDP communication via **Ethernet** between the FPGA and the host PC.
Experimental results: Test Data

The performance of the reconfigurable Wavelet Denoiser has been assessed using public available datasets of simulated neural signals, constructed starting from a database of real physiological spikes.

The background noise overlapped to the significant signal is obtained considering spikes of different neuronal cells at random times and amplitudes.

Sampling Frequency: 12kHz  Useful Bandwidth: 300Hz – 3kHz

Background noise: 0.1  Background noise: 0.3
Wavelet Denoiser parameters defined at runtime:

- \( N = 4 \) of decomposition/recomposition levels;
- the removal of the approximation signal at the 4\(^{th}\) decomposition level determining an output frequency bandwidth in the range of [375Hz-3kHz].
- \( b\_len = 500 \) samples as length of each input buffer frame;
- the Haar/ Daubechies 2 families as mother wavelets.
Accuracy: low level noise and *Haar* as mother wavelet
Accuracy: high level noise and *Haar* as mother wavelet
Accuracy: low level noise and Daubechies 2 as mother wavelet
Area occupancy and Power Consumption

- The datapath of the reconfigurable filter has been synthesized in order to evaluate the effectiveness of our approach in terms of area and power saving.

- We compared the Global Kernel assembled by the MDC tool with:
  - the datapath obtained by the 3 identified kernels without any resource sharing among them (Static Global Kernel);
  - the Cascaded Kernel implementing the wavelet denoising as a fully-parallel solution without sharing actors among the various decomposition/recomposition levels.

- Results for the Cascaded Kernel only represent an estimation taking into account the number of required FIR filters and the hardware resources correspondent to the various modules of the HDL components library.
Synthesis Results for *Multiplier* and *Adder* FUs

“Multiplier” and “Adder” FUs determine the largest contribution in terms of area and power consumption.

<table>
<thead>
<tr>
<th>Implementation</th>
<th>adders</th>
<th>multipliers</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDC Global Kernel</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>Static Global Kernel</td>
<td>6</td>
<td>4</td>
</tr>
<tr>
<td>Cascaded WD</td>
<td>20</td>
<td>32</td>
</tr>
</tbody>
</table>

*FPGA* and *ASIC* (using Cadence RTL Compiler targeting a 90nm CMOS library) synthesis results for the relevant FUs:

<table>
<thead>
<tr>
<th>FU</th>
<th>FPGA</th>
<th>ASIC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Slices</td>
<td>Flip Flops</td>
</tr>
<tr>
<td>adder</td>
<td>341</td>
<td>116</td>
</tr>
<tr>
<td>multiplier</td>
<td>138</td>
<td>131</td>
</tr>
</tbody>
</table>
FPGA synthesis results

- FPGA synthesis using the Xilinx FPGA Spartan-3E 1600 as target:

<table>
<thead>
<tr>
<th>Implementation</th>
<th>Slices [%]</th>
<th>Flip Flops [%]</th>
<th>MULT18x18s [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDC Global Kernel</td>
<td>14</td>
<td>5</td>
<td>22</td>
</tr>
<tr>
<td>Static Global Kernel</td>
<td>22</td>
<td>8</td>
<td>44</td>
</tr>
<tr>
<td>Cascaded WD</td>
<td>76</td>
<td>22</td>
<td>356</td>
</tr>
</tbody>
</table>

- The MDC Global Kernel is able to achieve 36% of saving in terms of slices compared to Static Global Kernel and 82% compared to the Cascaded WD solution.

- Considering the Xilinx multiplier primitives, the resource saving percentage is 50% and 97% respectively.
ASIC synthesis results

![Graph showing ASIC synthesis results with MDC Global Kernel, Static Global Kernel, and Cascaded WD compared to each other in terms of area and power. The graph indicates a 40% reduction in area and an 86% reduction in power for MDC Global Kernel, a 90% reduction in area for Static Global Kernel, and a 40% reduction in power for Cascaded WD.]
Results evaluation

- Provided that:
  - in the **MDC Global Kernel** case, the same resources are reused at each level;
  - in the **Cascaded Kernel** case, the number of required resources is linearly proportional to the number of levels;

the more will be the depth of the denoiser the larger will be the benefits of adopting the MDC-based approach.

- Strict temporal constraints would make impossible the minimization of hardware resources within kernels. In those cases, a compromise design choice must be done to balance resource saving and processing capacity.

- In other cases different kernel models, for example exploiting *pipelining* solutions, would be beneficial.
Conclusions

- In this paper, the implementation of a Wavelet Denoiser allows to demonstrate that:
  - the applicability of the MDC tool on a completely different application field compared to the original one it was conceived for;
  - a non-static implementation of a denoiser is possible leveraging a coarse-grained reconfigurable hardware design platform.

- System correctness and accuracy have been properly verified using a processor-coprocessor test environment and simulated neural signals as input data, varying the values assigned to the various parameters.

- The MDC-based solution is capable of an on-line processing of the incoming samples maximizing the resources reuse and determining area and power minimization.
Acknowledgement

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